

VLSI SYSTEM DESIGN

*Proceedings of the
Third International Workshop on
VLSI System Design*

Bangalore, India
January 6-9, 1990

Editors

L M Patnaik

*Indian Institute of Science
Bangalore, India*

A D Singh

*University of Massachusetts
Amherst, USA*

Sponsored by

**Indian Institute of Science
Department of Electronics, Government of India**



Tata McGraw-Hill Publishing Company Limited
New Delhi

McGraw-Hill Offices

New Delhi New York St Louis San Francisco Auckland Bogotá Guatemala
Hamburg Lisbon London Madrid Mexico Milan Montreal Panama
Paris San Juan São Paulo Singapore Sydney Tokyo Toronto

© 1990, TATA McGRAW-HILL PUBLISHING COMPANY LIMITED

No part of this publication can be reproduced in any form or by any means without the prior written permission of the publishers

This edition can be exported from India only by the publishers, Tata McGraw-Hill Publishing Company Limited

Sponsoring Editor: RANJAN KALL

Production Officer: B L DOSRA

Layout Artist: D D CHAUHAN

Published by Tata McGraw-Hill Publishing Company Limited,
4/12 Asaf Ali Road, New Delhi 110 002, and printed at
Rajkamal Electric Press, B-35/9 GT Karnal Road, Delhi 110 033

Preface

There is a concerted effort in India for promoting VLSI design due to the thrust given by the Department of Electronics, Government of India. As a first phase towards promoting this activity, VLSI design centres were set up at premier institutions, viz. Indian Institute of Science, Bangalore, Indian Institutes of Technology and the Central Electronics Engineering Research Institute, Pilani. The major activities of these centres include design and development of prototype VLSI tools which can be absorbed by the Indian industry. The government has also set up ten major VLSI design centres throughout the country to support the Indian electronics industry.

To discuss recent advances in VLSI system design, both in India and abroad, on a common platform, the First International Workshop was held at Madras in 1986 and the second at Bangalore in 1988. The interest generated by these Workshops has encouraged the Indian VLSI community to organize these meetings on a regular basis.

The present Third International Workshop is being held at Bangalore, India, during January 6-9, 1990. This Workshop is sponsored by the Indian Institute of Science, Bangalore, and Department of Electronics, Government of India and is co-sponsored by the Indian Telephone Industries, Bangalore, Gateway Design Automation (India) Private Limited, New Delhi, Hindustan Computers Limited, Wipro Information Technology Limited, the Computer Society of India, the IEEE India Council and the IEEE Bangalore Section. This volume is a collection of papers accepted for presentation at the Workshop.

The Coordinators are thankful to the organizers of the earlier Workshops, Dr H N Mahabala, Dr Ravi Apte, Dr V D Agarwal and Dr A Prabhakar for their suggestions and assistance. The secretarial and organizational assistance provided by Mrs G Bhanumathy, Mr K H Gowranga, Mr T K Sudarshan and Mr W Gowrishankar of the Microprocessor Applications Laboratory and several students of the Indian Institute of Science, Bangalore, is gratefully acknowledged. We also appreciate the help rendered by Mr R Ravichandran of Indian Telephone Industries.

L M Patnaik

A D Singh

Coordinators

L.M. Patnaik, IISc, Bangalore
A.D. Singh; U Mass, Amherst, USA

Programme Committee

J. Abraham, UT-Austin, USA
V.D. Agrawal, AT&T, USA
R. Apte, Valid Logic, USA
R. Brodersen, UC-Berkeley, USA
Chandra Sekhar, CEERI, Pilani
M.D'Abreu, GE, USA
M.M. Hasan, IIT, Kanpur
R.K. Iyer, U. Illinois, USA
A. Kumar, IIT, Delhi
H.N. Mahabala, IIT, Madras
D.A. Mohan, BEL, India
P. Pal Chaudhuri, IIT, Kharagpur
U.P. Phadke, DOE, New Delhi
A. Prabhakar, ITI, Bangalore
D.K. Pradhan, U Mass, Amherst, USA
V. Rajaraman, IISc, Bangalore
S.S.S.P. Rao, IIT, Bombay
S.M. Reddy, U. Iowa, USA
V.P. Srinu, UC-Berkeley, USA
V. Venkateswarulu, CDOT, Bangalore
A. Yamada, NEC, Japan
M.J. Zarabi, SCL, Chandigarh

Tutorial Coordinator

V.D. Agrawal, AT & T, USA

Local Organising Committee

Lalitha Harale, IISc, Bangalore
J. Mohan Kumar, IISc, Bangalore
N. Nagaraja Rao, IISc, Bangalore
M.K. Srinivas, IISc, Bangalore
S. Sundaram, IISc, Bangalore
T.G. Venkatesh, IISc, Bangalore
G.H. Visweswara, ITI, Bangalore

Contents

<i>Preface</i>	v
One LOGIC SYNTHESIS	1
Area Optimization Using Decoded PLA <i>G. Rajagopalan and M.M. Hasan</i>	3
HARP : A Hierarchical Approach to Area and Performance Optimization for Multi-Level Logic <i>Ajit M. Prabhu, David W. Tsao, Steven G. Rothweiler and Mario C. Lega</i>	8
Logic Design Using Pass-Transistors <i>Anura P. Jayasumana, Waleed Al-Assadi and Yashwant K. Malaiya</i>	13
ABS : An Automated Behavioural Synthesis System <i>C.A. Mandal and P. Pal Chaudhuri</i>	18
Two VLSI ARCHITECTURES	25
HIPERCAD : Parallel Algorithms for High Performance VLSI CAD <i>Prithviraj Banerjee</i>	27
A Low-Latency Crossbar Chip for Multiprocessors <i>Vason P. Srin</i>	33
Cache Memory Systems in the HP9000/HP3000 NMOS VLSI Processors <i>Jim Callister, Chuen Hu, Vighneswara R. Mokkarala and Dale Morris</i>	53
A Family of Reliable Systolic Correlators <i>Ravi Ramaswamy, Gavin Brebner and David Aspinall</i>	59
Three HIGH LEVEL SYNTHESIS	71
A Global Router for Gate-Arrays based on Karmarkar's Interior Point Methods <i>Ravi R. Pai, Narendra K. Karmarkar and S.S.S.P. Rao</i>	73
A Generic Channel Router for Gate Arrays <i>Anvind Savargaonkar and K.S. Raghunathan</i>	83
A Comparative Study of Techniques for Synthesis of Optimal Structures from Behavioral Descriptions <i>M. Balakrishnan and Anshul Kumar</i>	91
Automatic Synthesis of Data Paths based on the Integer Programming Algorithm <i>Janani Janakiraman and Biswadip Mitra</i>	97
Obstacle Enclosing Routing Algorithm <i>N.K. Hayathnagarkar and S.S.S.P. Rao</i>	103

Four	ARCHITECTURES/ALGORITHMS FOR CAD I	109
	Relaxation-Based Circuit Simulation on a Hypercube: Design, Simulation, and Performance Evaluation Studies <i>Srilata Raman</i>	111
	Search Parallelism in VLSI CAD Problems <i>Sunil Arvindam, Vipin Kumar, V. Nageshwara Rao and Vineet Singh</i>	119
	PMAZE : A Parallel Maze Routing for Hypercube Computers <i>R. Mall and L.M. Patnaik</i>	124
	Performance of Sparse Matrix Algorithm on a Transputer Based System <i>N. Seetharaman, M. Srinivas, A. Basu and A. Paulraj</i>	133
Five	TEST GENERATION & DFT	139
	Cellular Automata as a Built-in Self-Test Structure to Generate Pseudoexhaustive Test Pattern <i>Aloke K. Das and P. Pal Chaudhuri</i>	141
	PLATES : An Efficient PLA Test Pattern Generator <i>James Jacob and Nripendra N. Biswas</i>	147
	An Augmented PLA with Function Dependent Easily Derivable Test Set <i>Md. Abdul Mottalib and P. Dasgupta</i>	155
	Weighted Random Test Generation Using Signal Statistics <i>Anirban Dasgupta, Susanta Misra, P. Dasgupta and P. Pal Chaudhuri</i>	161
	A Methodology for the Design of Easily Testable DCVSL Circuits <i>Sandeep Pagey, S.D. Sherlekar and G. Venkatesh</i>	167
	A New Approach for Cellular Realisation of TSC Checkers for m-Out-of-n Codes <i>Ajit Pal</i>	173
	Testability Issues in the Design of a Gate-Array based Chip : A Counter-Based Technique for Testing of Embedded Combinational Blocks <i>Pushkal Yadav, Rohit Nayak, Ravi R. Pai, S. Seenivasagan and S.S.S.P. Rao</i>	179
Six	ARCHITECTURES/ALGORITHMS FOR CAD II	187
	A Parallel Algorithm for Coloring Interval Graphs with Applications to Gate Matrix Layout and Register Allocation <i>C.P. Ravikumar and S. Sastry</i>	189
	Hardware Routing Engine for VLSI <i>N.K. Hayatnagarkar and S.S.S.P. Rao</i>	195
Seven	VLSI CAD & SIMULATION	203
	STITCH : A Stitchable DRC and Extractor for a Multiprocessor Network <i>H.N. Mahabala, B.I.B. Madhav, P.W. Mantri and Vyas Krishnan</i>	205
	PRIDE : PRogrammable user Interface for a Design Environment <i>Mahesh Mehendale and M. Giridhar Krishna</i>	211

Delay Extraction in MOS Digital ICs <i>Navneet K. Jain, R.S. Rana and A.B. Bhattacharyya</i>	219
NAUTILUS : An Open Physical Design Environment Based on an Object Oriented Data Manager <i>P. Bondano, D Bonifas, A.A.Jerraya, A.Hornik and B.Courtois</i>	240
POSTERS	245
VLSI Architecture	
Efficient Procedure for Minimization of Fixed Polarity Expansions of EXOR Logic Arrays <i>M.R. Mukerjee, N.V. Babu and V.V. Raman Gopal</i>	247
Design of a Processor using Distributed Arithmetic for Transforms and Image Rotation <i>N.B. Chakrabarti, V.G. Pawar and T.V.K.H. Rao</i>	254
A Deflection Processor Unit for Digital TV <i>S.Uma Mahesh, H.N. Mahabala and J.P. Raina</i>	263
Architecture for a 32-bit Pipelined RISC Processor <i>K.R. Muralidhar and H.N. Mahabala</i>	268
A Systolic Design of BENES and Datamanipulator Network for VLSI Implementation <i>Rabi N. Mahapatra and Barun K. Kar</i>	275
Regular Interconnection Pattern between Arrays for Fast Computation of Discrete Hartley Transform <i>Anindya S. Dhar and Swapna Banerjee</i>	283
Floating Point Processor with Gate-Array Technology : A Preliminary Design <i>G.N. Rathna, M.K. Sridhar, K. Parthasarthy and S.K. Nandy</i>	289
A Microcoded RISC <i>H.N. Mahabala, K.V.S. Rama Murthy and S. Uma Mahesh</i>	295
Logic Synthesis	
Automated Synthesis of Combinational Circuits by Tree Networks of Multiplexers <i>R.K. Goyal and A. Pal</i>	300
GALP : A Layout System for 3 Micron CMOS Gate Arrays <i>V.S. Raghunath and Manjit Singh Wallia</i>	306
VLSI CAD and Simulation	
An Edge Based Design Rule Checker for IC Layouts <i>Anil Dikshit, Sandeep Aranake and A. Arun</i>	313
A Fast Method for Computation of Signal Delays and Waveform Bounds of an RC Mesh <i>Navneet K. Jain, V.C. Prasad and A.B. Bhattacharyya</i>	322

An Object Oriented Database for Computer Aided Design <i>T.K. Nayak and A.K. Majumdar</i>	326
PLAYER : A Search Efficient IC Layout Editor <i>P.V. Srinivas and V.K. Dwivedi</i>	331
A High Speed, Portable, Functional Simulation System for VLSI CAD <i>Shantanu Jha, Shyam S. Jagini, Biswadip Mitra and Kameshwar Rao</i>	342
VERICIN : A Mixed A/D Simulation Environment <i>Debashis Roy Chowdhury</i>	348
PLDL : Procedural Layout Design Language for VLSI Layout <i>S.D. Wagle and S.K. David</i>	354
A Theoretical Approach to Predict Hazards in Digital Circuits <i>S. Ravishankar and Lawrence Jenkins</i>	362
A 25ns 512x8 SRAM: First Design Experience of a Software Team <i>Sudip Nag, Rajiv Jain, V.R. Sudershan, Joy Chhugani, Champaka Ramachandran, Sujoy Mitra, Shobana Swamy, Loganath Ramachandran, Kameshwar Rao, C.Muthukrishnan, Mahesh Mehendale, Mohan Kumar, Gangadhar Burra and S.S. Mahant Shetti</i>	368
 Test Generation & DFT	
Parallel Memory Testing : A BIST Approach <i>D. Roy Chowdhury, I. Sen Gupta and P. Pal Chaudhuri</i>	373
Characterization of Cellular Automata (CA) and Its Application for On Chip Deterministic Test Pattern Generation <i>Susanta Misra, P. Pal Chaudhuri and S. Subramanian</i>	378
A Rule Based Design-For-Test (DFT) Checker <i>Soumitra De Sirkar</i>	384
 Author Index	 389

Author Index

- Ajit M. Prabhu 8
Ajit Pal 173
Aloke K. Das 141
Anil Dikshit 313
Anindya S. Dhar 283
Anirban Dasgupta 161
Anshul Kumar 91
Anura P. Jayasumana 13
Arun A. 313
Arvind Savargaonkar 83
- Babu N.V. 247
Balakrishnan M. 91
Barun K. Kar 275
Basu A. 133
Bhattacharyya A.B. 219, 322
Biswadip Mitra 97, 342
Bondono P. 240
Bonifas D. 240
- Chakrabarti N.B. 254
Champaka Ramachandran 368
Chuen Hu 53
Courtois B. 240
- Dale Morris 53
Dasgupta P. 155, 161
David Aspinall 59
David S.K. 354
David W. Tsao 8
Debashis Roy Chowdhury 348
Dwivedi V.K. 331
- Gangadhar Burra 368
Gavin Brebner 59
Giridhar Krishna M. 211
Gorai R.K. 300
- Hasan M.M. 3
Hayatnagarkar N.K. 103, 195
Hornik A. 240
- James Jacob 147
Janani Janakiraman 97
Jerraya A.A. 240
Jim Callister 53
Joy Chhugani 368
- Kameshwar Rao 342, 368
- Lawrence Jenkins 362
Loganath Ramachandran 368
- Mahabala H.N. 205, 263, 268, 295
Madhav B.I.B. 205
Mahant Shetti S.S. 368
Mahesh Mehendale 211, 368
Majumdar A.K. 326
Mall R. 124
Mandal C.A. 18
Manjit Singh Wallia 306
Mantri P.W. 205
Mario C. Lega 8
Mohan Kumar 368
Mottalib Abdul Md. 155
Mukerjee M.R. 247
Muralidhar K. R. 268
Muthukrishan C. 368
- Nageshwara Rao V. 119
Nayak T.K. 326
Nandy S.K. 289
Narendra K. Karmarkar 73
Navneet K. Jain 219, 322
Nripendra N. Biswas 147
- Pai A. 300
Pal Chaudhuri P. 18, 141, 161, 373, 378
Parthasarathy K. 289
Patnaik L.M. 124
Paulraj A. 133
Pawar V.G. 254
Prasad V.C. 322
Prithviraj Banerjee 27
Pushkal Yadav 179
- Rabi N. Mahapatra 275
Raghunath V.S. 306
Raghunathan K.S. 83
Raina J.P. 263
Rajagopalan G. 3
Rajiv Jain 368
Rama Murthy K.V.S. 295
Raman Gopal V.V. 47
Rana R.S. 219
Rao S.S.S.P. 73, 103, 179, 195

Rao T.V.K.H. 254
Rathna G.N. 289
Ravi R. Pai 73, 179
Ravi Ramaswamy 59
Ravi Kumar C.P. 189
Ravishankar S. 362
Rohit Nayak 179
Roy Chowdhury D. 373

Sandeep Aranake 313
Sandeep Pagey 167
Sastry S. 189
Seenivasagan S. 179
Seetharaman N. 133
Sen Gupta I. 373
Shantanu Jha 342
Sherlekar S.D. 167
Shobana Swamy 368
Shyam S. Jagini 342
Soumitra De Sirkar 384
Sridhar M.K. 289
Srilata Raman 111
Srini Vason P. 33

Srinivas M. 133
Srinivas P.V. 331
Steven G. Rothweiler 8
Subramanian S. 378
Sudershan V.R. 368
Sudip Nag 368
Sujoy Mitra 368
Sunil Arvindam 119
Susanta Misra 161, 378
Swapna Banerjee 283

Uma Mahesh S. 263, 295

Venkatesh G. 167
Vighneswara R. Mokkarala 53
Vineet Singh 119
Vipin Kumar 119
Vyas Krishnan 205

Wagle S.D. 354
Waleed Al-Assadi 13

Yashwant K. Malaiya 13