ELEC 4200 Lab#12
PicoBlaze-Controlled Display System

AUBURN UNIVERSITY

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- References you may need:
  - *PicoBlaze KCPSM6 User Manual*
  - *PicoBlaze 8-bit Embedded Microcontroller User Guide*

Overview

- For this project you are going to implement and extend the multiplexed display system (LAB 7) with *PicoBlaze*.
- You are to modify your *PicoBlaze* system VHDL model(s) and assembly language program from the last three labs to implement this system.
- You can use any combination of modules in a hierarchical design to complete this, but the control system for the multiplexed display must be implemented in *PicoBlaze*.

Specifications

- User input for *PicoBlaze*-Controlled Display System
  - To be provided via the interrupting input port from Lab 11.
  - To be accessed as a 7-bit input port

- Interface circuitry for *PicoBlaze* to 7-segment display
  - Use output port design from Lab 10.
  - Two 8-bit registers, enabled by *PicoBlaze* WRITE STROBE and appropriate port IDs, to hold 7-segment values plus 8 display enable signals.
  - **Note:** Only one display enable signal should be active at a time.

- *PicoBlaze* program functional specifications
  - Interrupt routine takes 4-bit HEX data and 3-bit address from the input port and stores the data in one of eight registers or scratchpad locations, as specified by the 3-bit address.
  - **Note:** Display data can be updated any time via input port interrupts
  - Decodes HEX data to 7-segment display data.
  - Passes 7-segment data to the display, via output ports, to enable a digit sequence to continuously display eight independent values.

Advanced Design Options

- *Advanced Design*
  - In addition to the regular system specifications, *PicoBlaze* displays “ELEC4200" before displaying the eight input-port-provided 7-segment display values for 4 seconds, then the sequence repeats

- ***Super Design***
  - “ELEC 4200" scrolls across display between displaying the eight input-port-provided 7-segment display values for 4 seconds

Pre-lab Assignment

- Study *PicoBlaze* architecture and instruction set
  - Start your *PicoBlaze* program
  - Note: the brightness of the display of the individual digits is a function of how often and how long a given 7-segment display is being driven by the processor, which must be managed in the program

- Write/revise VHDL models as needed for:
  - Interrupting input port
  - Output port
  - *PicoBlaze* to 7-segment display interface circuitry
  - Top level model to interconnect *PicoBlaze* and other models (you choose the hierarchical architecture)

Lab Exercise

- Assemble your verified program via *KCPSM6.exe*
- Adjust your top-level PicoBlaze system as necessary
- Use Active-HDL to simulate and verify, as much as possible, your top-level VHDL model and program
- Synthesize, download, and verify your complete design on the NEXYS 4 DDR board
- Demonstrate your complete design to the GTA

Report Guidelines

- Be sure to include all sections required by the lab manual guidelines. In addition, be sure your report includes the following:
  - A description of the design you chose (regular, advanced, super) and why
  - A block diagram of your design
  - A description of the various levels of simulation and synthesis you did and why.
  - A discussion of your final test procedure and observed behavior
  - A discussion of what went right and wrong in your approach to design and design verification
  - A discussion of what you would have done differently if you were starting over with this particular project.
  - Your VHDL models and *PicoBlaze* programs should be included in the this report and referred to in your discussion.

Final Project Grades

- Weight of the final project grade = 2x the weekly labs
  - Demonstration grade = 60 points (max)
  - Final report grade = 40 points (max)
  - Total project grade = 100 points (max)

- Extra credit points (one "bonus" per student):

  Either

  - Up to 10 points added for correct "advanced design"

  or:

  - Up to 20 points added for correct "super design"