IEEE Solid-State Circuits Technology Workshop on CMOS Imaging Technology

San Fransisco Marriott Hotel
Wedensday, 7 February 1996

Organizing Committee

Xavier Arreguit, Centre Suisse D'Electronique et de Microtechnique SA

Alex Dickinson, AT&T Bell Laboratories

Lisa Dron, Northeastern University

Eric Fossum, Jet Propulsion Laboratory

Yoshiro Fujita, Japan Broadcasting Corporation (NHK)

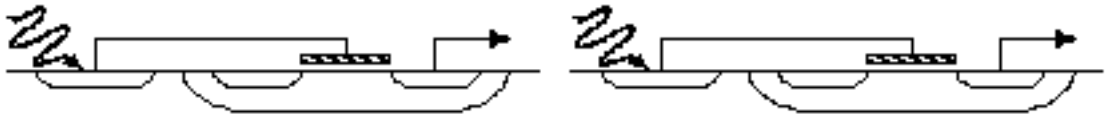
Dan McGrath, Polaroid Corporation

Phillip Wong, IBM Thomas J. Watson Research Center

Woodward Yang, Harvard University

Local Arrangements Anne Verfurth, Courtesy Associates

Solid State Circuits Council Liason Stan Schuster, IBM



Why did we ask you here?

- **2-d image arrays in a CMOS process technology appear practical & cost-effective**
- **They present interesting device problems, but they present even more interesting circuit problems**
- **There are a variety of possibilities to do imaging & to build on the imaging function**
- **Its time to discuss the "nuts & bolts" of CMOS imaging technology**

What are CMOS Image Sensors?

- Image sensors built in a CMOS process (or a CMOS process with enhancements) & which behave like CMOS circuits
- For historical background: Fossum, IEDM95

An Observation

CMOS imaging technology moves imaging from being a device problem to being a circuits problem

---

IEEE Solid-State Circuits Technology Workshop on CMOS Imaging Technology

San Fransisco Marriott Hotel
Wedensday, 7 Februarv 1996

Aren't all CMOS imagers the same?

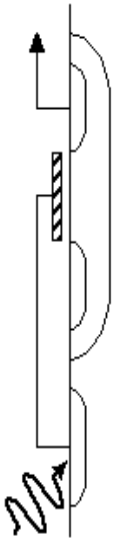
- **A CMOS process can be optimized for digital, for analog, for low power, for memory, or (if absolutely necessary) for imaging**
- **A CMOS pixel can be passive (photosite & switch) or active (photosite, active device & switches), can use a photodiode or a photogate, can have low impedance or high impedance, can be integrating or sampled, can be ...**
- **A CMOS imaging device can be integrated with on-chip processing**
- **A CMOS image sensor can perform well or can perform badly**

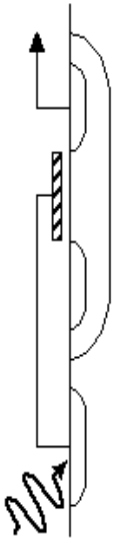
The Challenge:

To look at the diversity and pick out viable products

IEEE Solid-State Circuits Technology Workshop on CMOS Imaging Technology

San Fransisco Marriott Hotel
Wedensday, 7 Februarv 1996





Agenda

8:00 Continental breakfast & registration

8:45 Welcome, Stan Schuster, Solid States Circuits Council

8:50 Introductory comments, Dan McGrath, Polaroid Corporation

9:00 **Operation & analysis of CMOS active pixel sensors**, Bedabrata Pain, JPL

9:40 **Building & comparing passive & active pixels**, Peter Denyer, VLSI Vision Limited

10:20 Break

10:50 **Large area array with non-linear active current-mode pixels**, Vince Clark, Polaroid Corporation

11:30 **Fixed-pattern noise reduction techniques in CMOS imaging arrays**, Steve Decker, MIT

12:10 Lunch

1:45 **A 1024x1024 CMOS active pixel image sensor**, Alex Dickinson / Marc Loinaz, AT&T Bell Labs

2:25 **Color signal processing for CMOS active pixel sensor**, David Gibbons, AT&T Bell Labs

3:05 Break

3:40 **Analog CMOS implementation of low-level vision chips for low-power & real-time applications**, Xavier Arreguit, CSEM

4:20 **Technology & device scaling considerations for CMOS imagers**, Hon-Sum Philip Wong, IBM

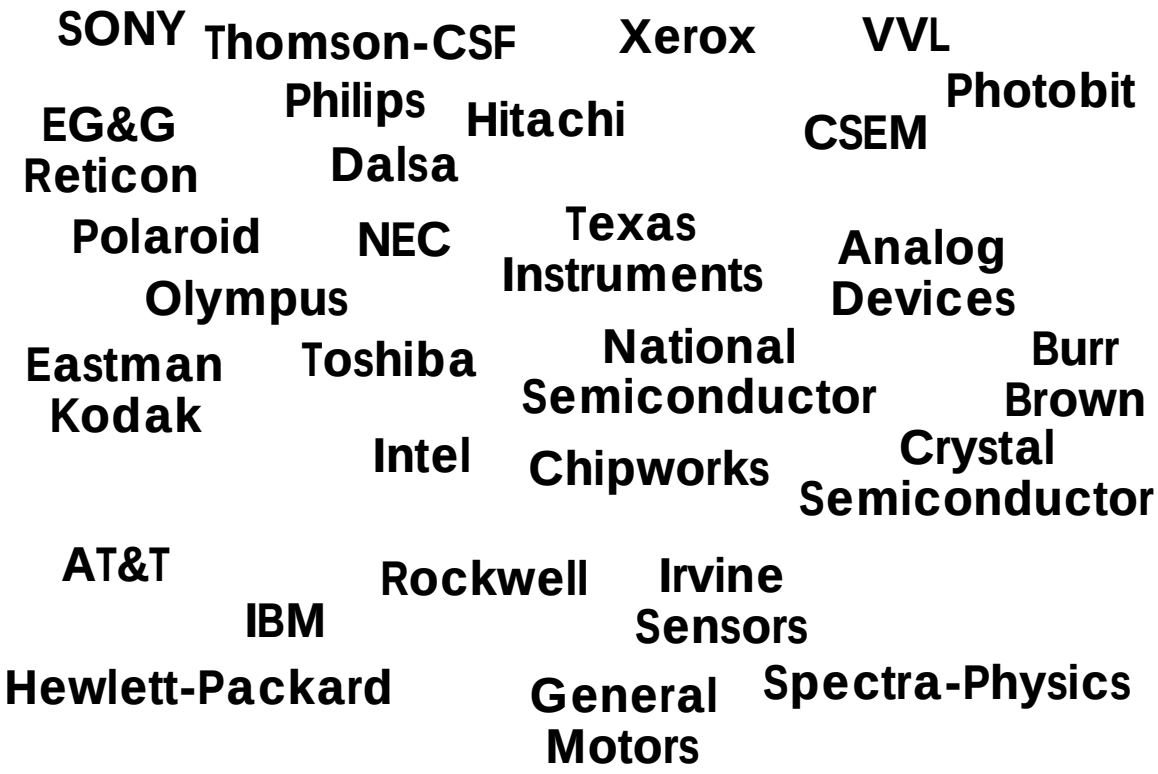
5:00 **Refreshments & Discussion**, Alex Dickinson, AT&T Bell Labs

n.b., talks are 30 minute followed by 10 minutes of discussion

---

IEEE Solid-State Circuits Technology Workshop on CMOS Imaging Technology

San Fransisco Marriott Hotel
Wedensday, 7 February 1996



IEEE Solid-State Circuits Technology Workshop on CMOS Imaging Technology

San Fransisco Marriott Hotel
Wedensday, 7 Februarv 1996