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Microelectronic Engineering xxx (2007) xxx–xxx

MICROELECTRONIC ENGINEERING

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Controlling resist thickness and etch depth for fabrication of 3D structures in electron-beam grayscale lithography

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Received 22 January 2007; accepted 13 February 2007

Abstract

In many applications such as optoelectronic devices, three-dimensional (3D) structures are required. Examples include photonic band gap (PBG) crystals, diffractive optical elements, blazed gratings, MEMS, NEMS, etc. It is known that the performance characteristics of such structures are highly sensitive to their dimensional fidelity. Therefore, it is essential to have a fabrication process by which such 3D structures can be realized with high dimensional accuracy. In this paper, practical methods to control thickness of the remaining resist and etch depth, which may be employed for fabrication of such 3D structures using grayscale electron-beam lithography, are described. Through experiments, explicit control of the remaining resist thickness and etch depth at the resolution of 20 nm for the feature sizes of 0.5 μm and 1 μm has been successfully demonstrated. Also, the 1:1 ratio of silicon to resist etching rates was achieved for transferring the remaining resist profile onto the silicon substrate.
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Keywords: Dose Control; E-beam lithography; Grayscale lithography; Nanoscale; Reactive ion etching; Remaining resist profile; Three-dimensional structures

1. Introduction

There are many applications, including optical devices, where multi-level or 3D structures are required. Performance characteristics of such devices are highly sensitive to dimensional accuracy of the structures. Therefore, it is essential to achieve high dimensional fidelity in the fabrication process. Various methods were developed for realizing 3D structures in the past.

The idea of micromachining was employed in several different ways including ultrasonic machining [1], laser machining [2], etc. They were mainly applied to fabricating holes of various shapes via selective etching and the feature size was O(10) to O(100) μm where O( ) denotes *in the order of*. Also, each method needed a special experimental set-up and was limited in speed.

More recently, a hole-area modulation method (MEMSNAS: Mircoloading effect for micromachining 3D structures of nearly all shapes) was designed for fabrication of grayscale structures of “nearly all shapes” [3]. The substrate is etched (RIE) through a mask which consists of a number of holes at square grid points. The etching rate of a substrate region depends on the size of holes above it. Again, only the feature size of O(1) or larger was considered.

Micro-stereolithography is a fabrication process which realizes 3D structures by solidifying the liquid monomer in a layer by layer fashion [4]. It involves a time-consuming repetitive process due to its layer-by-layer approach especially when the number of layers is large. The feature size in the structures fabricated by this technique was O(100) μm. Also, it is not applicable to typical substrates such as silicon.

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0167-9317/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2007.02.015

A more flexible approach to fabrication of 3D structures (especially grayscale 3D structures) is to employ *grayscale lithography*. A typical process may consist of two steps: transferring a structure onto the resist as the remaining resist profile and then etching the substrate through the remaining resist (if the final structure is to be in the substrate). For the first step, one may employ photolithographic (*grayscale photolithography*) or electron-beam (e-beam) lithographic (*grayscale e-beam lithography*) process.

In grayscale photolithography, the amount (intensity) of light transmitted through a mask, on which the remaining resist profile depends, is spatially controlled. An example of controlling the transmitted light is to vary the ratio of opaque (pixel) area to transparent area in the mask [5]. Another grayscale photolithographic technique, but not requiring the etching process, employs the high energy beam sensitive (HEBS) grayscale mask on top of the sol–gel thin film coated over the substrate and 3D structures are transferred onto the sol–gel layer [6]. Fabrication of grayscale structures such as blazed grating and Fresnel lens by these methods has been demonstrated. The grating width was mostly $O(10) \sim O(100)$ μm.

Grayscale e-beam lithography has the following advantages over the grayscale photolithography: (i) it does not require any mask and (ii) it has a good potential to achieve higher spatial resolution, at the expense of low throughput. In fact, 3D structures may be fabricated using the *binary* e-beam lithographic process multiple times, i.e. once for each depth. However, it suffers from a long total process time, the alignment problem between processes and a high cost, especially when the number of different depths is greater than two. *Grayscale* (e-beam) lithography can eliminate these drawbacks since it requires only one step of e-beam lithographic process.

As the first step toward developing a grayscale e-beam lithographic process for fabrication of nanoscale (100 nm or below) 3D structures, this study focuses on explicitly controlling, feature by feature, thickness of the remaining resist after development in the e-beam lithographic process and etch depth in the subsequent etching process. Thickness control of the remaining resist is achieved by determining a proper level of energy deposited (*exposure*) for each feature (thickness) in a given 3D structure. Given an exposure distribution to be achieved for the structure, the grayscale proximity effect correction scheme developed earlier [7] is employed to compute the energy to be given (*dose*) to each feature. An etch depth is realized by controlling the ratio of the substrate (Si) to resist etching rates. In this study, the two feature (step) sizes considered for staircase structures were 0.5 μm and 1.0 μm, and the depth resolution (step height) achieved was 20 nm. One of the goals in the etching process was to achieve the 1:1 ratio of the silicon to resist etching rates, which allows for transferring the remaining resist profile onto the silicon substrate without vertical scaling. No vertical scaling makes it possible to optimize the developing and etching processes independently. Nevertheless, the vertical scaling may be desirable in some applications.

In this paper, the procedures for determining dose to be given to each feature in a 3D structure to obtain the desired exposure distribution and achieving the 1:1 ratio of the silicon to resist etching rates to transfer the remaining resist profile onto silicon without scaling are described. Also, experimental results obtained for staircase structures are presented with detailed discussion.

2. Mapping functions

Two *mapping functions* may be employed to model the fabrication process using grayscale e-beam lithography, one for the e-beam lithographic step and the other for the etching step. Let f and g denote the two functions. The function f relates exposure to resist development depth, i.e. $R = f(E)$ where E is the exposure and $R = T_o - T$ where T_o and T are the initial and remaining thicknesses of resist, respectively. Note that f is an increasing function which may be estimated through experiments and calibrations. In Fig. 1, a 3D structure of staircase which is employed to investigate feature depth control is shown. The function g relates thickness of the remaining resist to etch depth, i.e. $S = g(T)$ where S denotes the etch depth. g is also an increasing function and is dependent on the etching rates of resist and substrate. Given the remaining resist thickness T, the etch depth S depends on the ratio of the two etching rates and the etching time. In this study, derivation of an explicit g was not attempted (refer to Section 4).

3. E-beam lithographic process

3.1. Dose determination

In order to determine dose to be given to each feature (e.g. a step in the staircase), the exposure level required for the feature is to be estimated first. The main focus of this study is on depth control, not CD (feature width and length) control. Therefore, dose control within each feature by partitioning it into regions is not considered. The function $R = f(E)$ may be estimated through curve fitting with experimental results. In Fig. 2, a set of experimental results

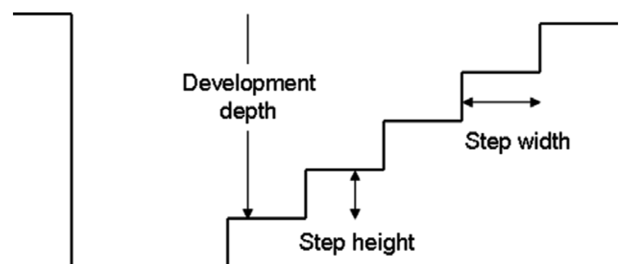

Fig. 1. A staircase structure consisting of 5 steps: when it is transferred onto resist, the development depth refers to the initial thickness of resist minus the remaining thickness of resist.

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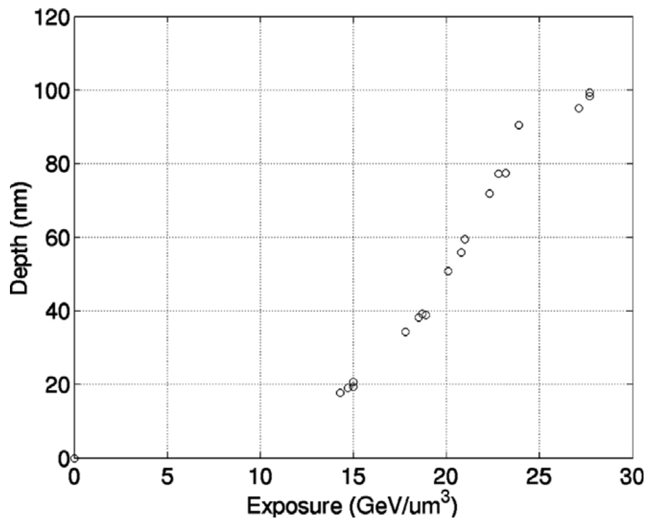

Fig. 2. Relationship between exposure and development depth for the staircase structure (step width of 1.0 μm) transferred onto 100 nm PMMA on Si with the beam energy of 50 keV.

is used to derive the relationship between the development depth and exposure. A curve may be fitted to these sample points in the graph such that a certain measure of error such as the mean square error is minimized. The curve is referred to when determining the exposure level for a given development depth. Then, dose for each step in the staircase structure is computed by the grayscale proximity effect correction program PYRAMID [7].

3.2. Development process

The silicon wafers were spin-coated with the PMMA (polymethylmethacrylate) 495/11A diluted with anisole solution at various speed from 3000 to 4000 rpm for 55 s, to obtain the resist thickness of 100 nm. Then, the samples were baked at 180 °C for 3 min. Resist thickness was measured by the Filmetrics thin-film measurement system. The staircase patterns were exposed using a JEOL 6000 FS/E direct-write electron-beam lithography tool, which is operated at 50 keV. After exposure, the resist was developed in the methylisobutyl ketone (MIBK): IPA (isopropyl alcohol) = 1:3 developing system for 60 s and IPA for 30 s at 21 °C.

4. Etching process

Typical reactive ion etching process is mainly controlled by three process factors, i.e. RF power, gas pressure, and gas composition. Optimization of the three factors usually requires a large number of experiments and error analysis. In order to reduce the number of experiments, one may make use of the Taguchi design of experiment (DOE) to determine dependency of etching process on the three factors first and then guide subsequent experiments according to the dependency [8,9].

The staircase structure was transferred onto the silicon substrate by etching, using Trion Technology Oracle RIE tool, through the remaining resist, of which profile resembles the structure. That is, the remaining resist was used as a grayscale etch mask which is also etched. The thick-

Table 1
Taguchi DOE for optimizing RIE process

No.	Factors			Responses		
	RF power, W	Pressure, m torr	O_2, sc cm	Si E/R[a], nm/s	PR E/R[b], nm/s	Rt Si/PR[c]
1	100	50	0	2.25	3.70	0.61
2	100	100	5	1.74	4.48	0.39
3	100	150	10	1.31	5.03	0.26
4	150	50	5	3.84	5.87	0.65
5	150	100	10	3.18	6.86	0.46
6	150	150	0	3.01	6.70	0.45
7	200	50	10	4.69	10.12	0.46
8	200	100	0	9.23	7.88	1.17
9	200	150	5	8.16	8.49	0.96

[a] Si E/R: silicon etching rate.
[b] PR E/R: PMMA resist etching rate.
[c] Rt Si/PR: the ratio of the silicon etching rate to the PMMA etching rate.

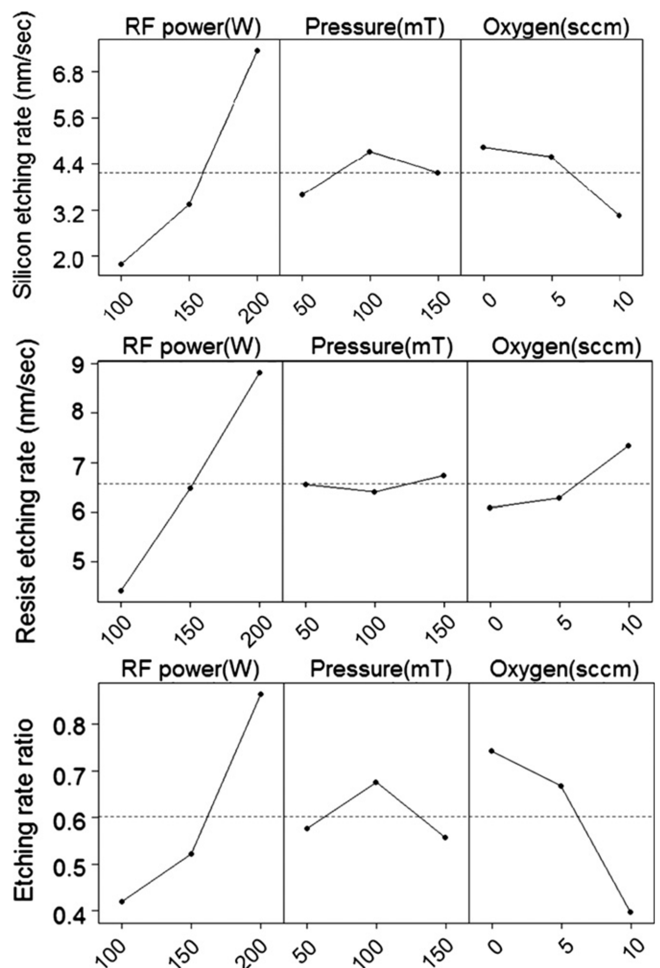

Fig. 3. Effect of RF power, pressure, and gas composition on the etching rates of silicon and PMMA, and the ratio of the silicon etching rate to the PMMA etching rate.

ness of remaining resist of a feature (step) determines when the silicon substrate area corresponding to the feature starts to be etched and the depth of the etched feature depends on the ratio of resist and silicon etching rates. Initial experiments were designed according to the DOE which consisted of three levels for the three process factors. The active gases used for etching were O_2 and SF_6 where the SF_6 flow rate was 45 sc cm with the O_2 flow rate varied.

Effects of the three process factors on the etching rates of silicon and PMMA and their ratio are provided in Table 1. Through statistical analysis of the data in Table 1, tendency of responses for each factor is estimated as shown in Fig. 3 where it can be seen that both the individual etching rates and their ratio show a strong dependency on RF power and oxygen flow rate. As the oxygen flow rate increases, the silicon etching rate decreases since the silicon surface becomes oxidized. As expected, the resist (PMMA) etching rate increases as the oxygen flow rate increases. When the RF power level is low, the etching rate of silicon is lower than that of PMMA. This may be explained, under the assumption of the same reactivity for both silicon and PMMA, by the fact that the volume per mole is smaller for silicon than for PMMA and each silicon atom needs 4 F radicals to form volatile products. Also, the microloading effect is observed, i.e. the silicon etching rate was lowered as etching progressed [3,10]. For a relatively low RF power, the amount of active species is small and therefore the etching rate is limited by the transport rate of active species. As the area of exposed silicon increases, the rate at which the active species are supplied to the silicon area doesn't scale up linearly, leading to a lower silicon etching rate. As the RF power is increased into the range shown in Fig. 3, it appears that the microloading effect becomes insignificant and the 1:1 ratio of the silicon to resist etching rates is achievable. When the RF power is higher, more active species are generated and, therefore, the silicon etching rate is limited not by the transport rate, but by reaction between silicon surface and active species. Hence, the microloading effect diminishes. Also, the energy associated with ion bombardment is higher for a higher RF power, increasing the silicon etching rate more than the PMMA etching rate thanks to the weaker bond of silicon, and in turn enabling the 1:1 ratio of the silicon to resist etching rates in the region of high RF power and low oxygen flow rate.

A few combinations of the three process factors, selected based on the tendencies in Fig. 3, were tried. The recipe RF power of 200 W, pressure of 100 m torr and oxygen flow rate of 2 sc cm resulted in an etching rate ratio very close to 1:1 and the best etched silicon profile. The etching rate of silicon was 9.48 and 8.97 nm/s for the staircase structures with the step width of 1.0 μm and 0.5 μm, respectively, and the PMMA etching rate for both structures was 8.72 nm/s.

5. Experimental results

In Figs. 4 and 5, the remaining resist and etched silicon profiles obtained for the staircase structures are provided,

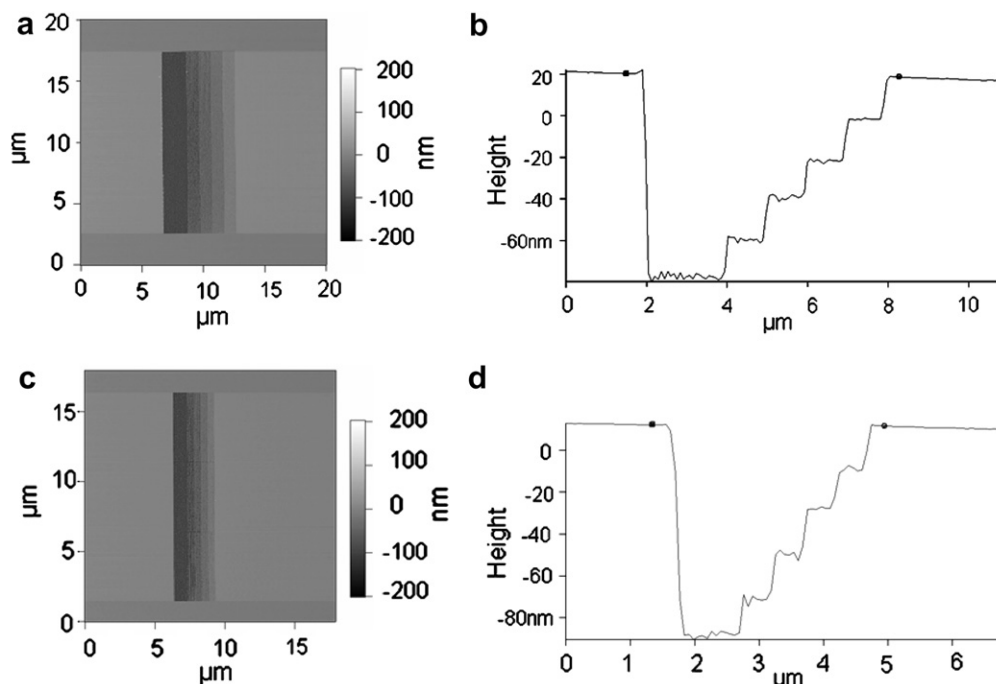

Fig. 4. The remaining resist profiles, after development, of the staircase structures transferred onto PMMA on Si when the step width is 1.0 μm ((a) top view and (b) cross-section: the left-most step is 2 μm wide) and 0.5 μm ((c) top view and (d) cross-section: the left-most step is 1.0 μm wide). The step height is 20 nm. Note that the height and width are plotted in different scales in (b) and (d).

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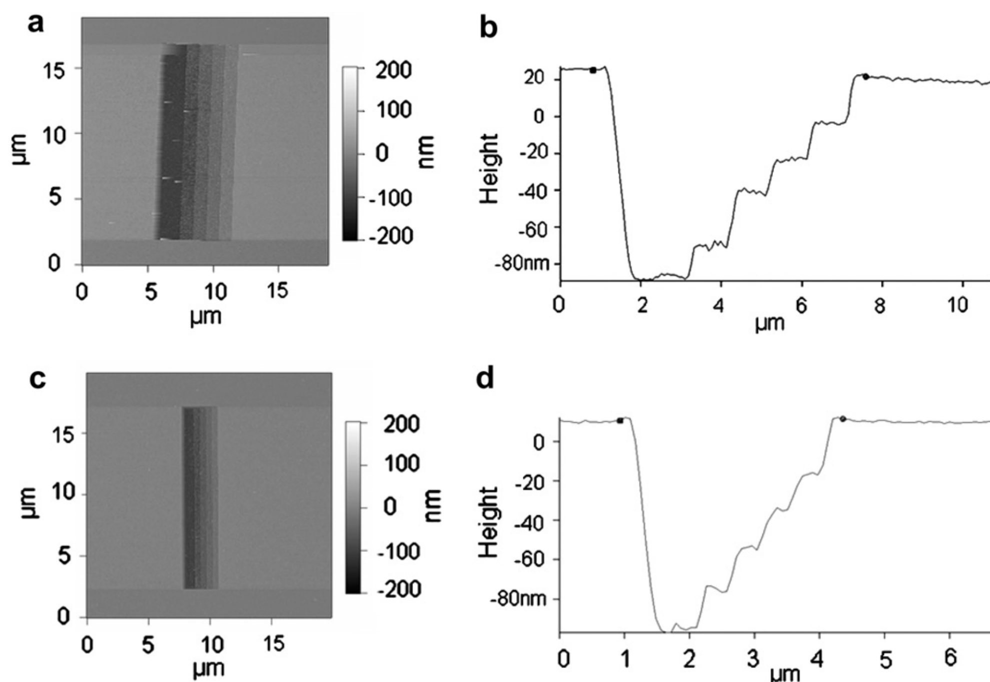

Fig. 5. The etched pattern profiles of the staircase structures transferred into Si when the step width is 1.0 µm ((a) top view and (b) cross-section: the left-most step is 2 µm wide) and 0.5 µm ((c) top view and (d) cross-section: the left-most step is 1.0 µm wide). Note that the height and width are plotted in different scales in (b) and (d).

which were measured by the Asylum MFP-3D atomic force microscope (AFM). A surface profiler, which is normally employed for measuring the etching profile, could not be used due to the very small feature size (step width) in the staircase structures. Two staircase structures with different step widths, i.e. 0.5 and 1.0 µm, were considered. The step height is 20 nm in both structures. The doses for different steps in each staircase structure were computed based on the exposure-depth relationship in Fig. 2.

In Fig. 4, it is seen that the five steps of the staircase structures are well separated in the resist profile and the step heights are uniform. The average percentage error (difference) between the ideal and actual depths of steps in the remaining resist profile is no greater than 2.5% in both staircase structures. Here, the actual depth is an averaged measure since each step is not completely flat.

In Fig. 5, it can be observed that the remaining resist profiles of the staircase structures have been successfully transferred onto silicon. However, compared to the resist profiles, the etched silicon profiles show some degradation of the staircase structure as can be seen in Fig. 5b and d, i.e. edge smoothing (smaller edge slope and corner rounding). This degradation is believed to be due to the fact that the RIE process employed may not be completely anisotropic. The lateral component of etching would make the edge slopes smaller in the etched profile. This also contributes to rounding the corners by making the corners etched faster than their surroundings. Another observation is that the entire staircase structures are shifted down about 10 nm and 5 nm in the structures with step width of 1.0 µm and 0.5 µm, respectively. Ignoring this shift (which is most probably due to over-etching), the percentage step depth error is less than 2.1% for the two structures.

6. Summary

In this study, the issue of controlling feature depth in grayscale e-beam lithographic and etching processes has been addressed. For the e-beam lithographic process, dose to be given to each feature is derived from the exposure-depth mapping function by using the grayscale e-beam proximity effect correction scheme (PYRAMID). The etching process is guided by controlling the etching rates of the resist (PMMA) and silicon substrate such that the desired structures are eventually transferred onto the substrates. Through experiments using staircase structures with step width of 0.5 µm and 1.0 µm, it has been shown that depth control in the resolution of 20 nm and the 1:1 ratio of the silicon to resist etching rates are achievable. The percentage error of step depth in the two staircase structures considered is less than 2.5% in the e-beam lithographic process and less than 2.1% in the final etched silicon profiles.

The current and future efforts include consideration of smaller features (step width), optimization of the e-beam lithographic and etching processes, etc.

Acknowledgements

This study (University of Tennessee) was in part supported by SRC. Jung–Won Park at ORNL helped with

etching process. The AMSTC (Alabama Microelectronics Science and Technology Center) provided a travel grant.

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