ELEC 5280/6280/6286 – BUILT-IN SELF-TEST  
(Elective for ECPE, Elective for ELEC)

Proposed Catalog Data:  
ELEC 5280/6280/6286. BUILT-IN SELF-TEST (3) LEC. 3. Pr., ELEC 2200, ELEC 2210. Testing during product life-cycle, fault models and detection, design for testability, test pattern generation, output response analysis, concurrent fault detection, manufacturing and system use, built-in self-test approaches and applications.

Textbook:  

References:  

Coordinator:  
Charles E. Stroud, Professor of Electrical & Computer Engineering

Course Objectives:  
1. An understanding of the testing process and its impact on design and manufacturing.
2. An understanding of fault modeling, detection, and simulation techniques.
3. The ability to generate test patterns to detect faults and fault models in a digital circuit.
4. The ability to implement Built-In Self-Test techniques including test pattern generators, output response analyzers, test controllers, and input isolation mechanisms.
5. Hands-on experience with Computer-Aided Design (CAD) tools for fault simulation.

Prerequisites by topic:  
1. Digital logic design and analysis or switching theory
2. Electronics and MOS transistors

Topics:  
1. Overview of Built-In Self-Test (BIST)  (2 classes)
2. Fault models, detection, and simulation  (6 classes)
3. Design for testability  (3 classes)
4. Test pattern generation  (5 classes)
5. Output response analysis  (2 classes)
6. Concurrent fault detection  (2 classes)
7. Manufacturing and system level use of BIST  (2 classes)
8. Built-in logic block observer  (2 classes)
9. Pseudo-exhaustive BIST  (2 classes)
10. Circular BIST  (2 classes)
11. Scan-based BIST  (3 classes)
12. Non-intrusive BIST  (2 classes)
13. BIST for regular structures  (3 classes)
14. BIST for programmable logic  (3 classes)
15. Mixed-signal BIST  (3 classes)
16. Exams and review  (3 classes)

Typical methods for evaluating student performance:  
Hour quizzes (3)  60%
Final exam  20%
Homework/design projects  20%

Graduate students will be assigned additional and more complex design projects than undergraduate students (see Homework/Design Projects below for more details). In addition, graduate students will be given additional and more complex exam questions than undergraduate students. For graduate students, the grading scale will be: 90%-100%=A, 80%-89%=B, 70%-79%=C, and 69% and below = F. For undergraduate students, the grading scale will be: 90%-100%=A, 80%-89%=B, 70%-79%=C, 60%-69%=D, and 59% and below = F
Homework/Design Projects: Design projects will include implementation, simulation, and evaluation of Built-In Self-Test approaches in internationally recognized and accepted benchmark circuits (such as the International Society on Circuits and Systems or the International Test Conference). These set of benchmark circuits provide a range in complexity and, as a result, assignment of these benchmark circuits for design projects will be based on complexity and academic standing with PhD students assigned the more complex circuits, MS students assigned less complex circuits, and undergraduate students assigned the least complex circuits. Graduate students will be assigned additional and more complex design projects than the undergraduate students in order to obtain a more in-depth understanding of (and more refined skills associated with) the various Built-In Self-Test approaches and techniques. Finally, graduate students will be assigned related technical papers from journals and international conferences for extended learning from which they will either give a short oral presentation to the class on their assigned topic, or write a report to be turned in by the end of the semester as part of their homework/design project score.

Academic Honesty: Students are expected for pursue their academic work with honesty and integrity according to the University Academic Honesty Code which may be found in the SGA Code of Laws cited in the Tiger Cub. Violations of this principle will be reported to the Academic Honesty Committee.

Computer usage: Fault modeling and simulation assignments will require the use of the digital logic fault simulation program AUSIM, available for free on the web page www.eng.auburn.edu/~strouce/ausim.html. Note that every student is expected to do his/her own work. Computer-aided design implementations and evaluations of Built-In Self-Test approaches will be performed using various support programs also available at the above web page. Discussion of various aspects of the problems/design projects with fellow students is acceptable, provided that solutions/designs are not copied.

Class attendance: Students are expected to attend class regularly and on time. In case of absence, the student is responsible for all course business conducted in class.

Policy on unannounced quizzes: There will be no unannounced quizzes.

Special Accommodations: Any student requiring special accommodations should meet with the instructor within the first week of classes, bringing their Accommodation Memo from the Program for Students with Disabilities (located at 1244 Haley Center, phone: 334-844-2096, open 7:45-11:45am and 12:45-4:45pm M-F).

Contribution of course to meeting the professional component
Engineering topics: 3 credits
33% engineering science (1 credit)
67% engineering design (2 credits)

Primary program outcomes related to this course:
Outcome 1. Ability to apply knowledge of math, science and engineering to solve problems.
Outcome 2. Ability to apply in-depth knowledge in one or more disciplines
Outcome 3. Ability to design an electrical component or system to meet desired needs.
Outcome 6. Proficiency in the use of computers and other modern tools to solve engineering problems.

Prepared by: Charles E. Stroud Date: November 24, 2008
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