Atmel’s AT94K Series
Field Programmable System Level
Integrated Circuit (FPSLIC)

Embedded Systems Based
Built-In Self-Test and Diagnosis
of the FPGA Core
System-On-Chip Issues

- $250K+ NRE
  - CES note: these are old numbers – much higher now

- $100K+ design tools
  - CES note: these are old numbers – much higher now

- Large volume requirements

- Custom product

- Long design time

- High risk

- IP issues (availability, cost implementation)

>> System level integration not viable for most customers
Field Programmable System Level Integrated Circuit
reducing power consumption

Most of power used in I/O pads

Power is reduced by more than 50%
- Standby <100μA
- Active 2-3mA/MHz
Atmel Programmable SLi Roadmap

- **AT40KxxAL** with **Low $**
- **AT40K with RISC uC**
  - **AVR™ FPSLIC™**
- **AT40KxxAV** with **Low $**
- **AT40K with ARM**
  - **ARM FPSLIC™**
- **AT40KxxAX** with **Low $**
- **1.8V 0.12u**
- **3.3V 0.35u**

**Features**

- **ASIC FPSLIC™ with Embedded AT40K FPGA core**

**Timeline:**
- **2000**
- **2001**
- **2002**
- **2003**
User-Defined Logic Spectrum

- **PAL-Type**
  - ATF22V10
  - ATF16V8
  - ATF20V8
  - **Decoders, Glue Logic**

- **CPLD**
  - ATV2500B
  - ATF1500 Fam
  - ATV750B
  - **State machines, Timing, Control**

- **FPGA**
  - AT6000
  - AT40K
  - **RAM/Logic, Computing, Co-processing**

- **FPSCI**
  - **Programmable SLI with AVR**
  - **High Volume/Low Cost**
  - System Level Integration

- **Gate Array**
  - **ATL25 Series**
  - **ATL35 Series**
  - **ATL50 Series**
  - **ATL60 Series**
  - **Macrocells 0.25, 0.35, 0.5, 0.6 Analog / Digital**

- **Cell based ASIC**
  - **Custom ASIC**
  - **Analog / Digital/NV Memory, RF**
  - **Total Customization Very High Volume**

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  - **System Level Integration**
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Atmel’s Flash MCU Families

Price vs Performance

- Engine Control
- Laser Printer
- Internet
- Settop Boxes
- Disk Drives
- Cellphones
- Auto Elect.
- Appliances
- Keyless Entry

Price

$1 $2 $5 $10 $20

Performance

AVR

C51

ARM-7
Monolithic SRAM Based FPSLIC

- Configurable SRAM
- Up to 36K bytes of SRAM
- AT40K FPGA
- From 5K to 40K gates FPGA

20 MIPS* - 8bit RISC MCU
120+ instructions
*30 MIPS version available Q4 2001
Designer Defined Program and Data SRAM Allocation

- Memory partition is user defined during development
- Easy to trade-off Program and Data SRAM

* 2K Words (x16) for μFPSLIC (AT94K05)
Internal Data SRAM Access

Data SRAM (DPRAM)
4K byte up to 16Kbyte

True Dual Port Access
AVR can disable writing from FPGA
FPSLIC Embedded Blocks

- Software configurable interface between blocks already implemented
- Pre-implemented Interface blocks save 2000-5000 FPGA gates
Internal I/O space and Interrupts

Write:
ldi r16,0x00
ldi r17,0x02
out FISCR,r16 ; I/O select 0
out FISUA,r17 ; r17 data on the bus
AVR-FPSLIC Family

- 5K, 10K and 40K gate AT40K FPGA options
- AVR microcontroller
  - 120+ instructions

<table>
<thead>
<tr>
<th>Device</th>
<th>Array Size</th>
<th>4-LUTs FFs</th>
<th>FPGA Gates</th>
<th>FreeRAMs SRAM bits</th>
<th>FPGA I/O</th>
<th>Program Memory Data SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT94K05</td>
<td>16x16</td>
<td>256</td>
<td>5K</td>
<td>16 RAMs 2048 bits</td>
<td>96 max</td>
<td>4K–16K Bytes/4K-16K Bytes</td>
</tr>
<tr>
<td>AT94K10</td>
<td>24x24</td>
<td>576</td>
<td>10K</td>
<td>36 RAMs 4096 bits</td>
<td>192 max</td>
<td>20K–32K Bytes/4K-16K Bytes</td>
</tr>
<tr>
<td>AT94K40</td>
<td>48x48</td>
<td>2,304</td>
<td>40K</td>
<td>144 RAMs 18432 bits</td>
<td>384 max</td>
<td>20K–32K Bytes/4K-16K Bytes</td>
</tr>
</tbody>
</table>
• AVR
  – Harvard architecture
  – 32 8-bit regs
  – ALU w/multiplier
  – 120+ instructions
FPSSLIC - Partial Reconfiguration using AVR

- Hardware implemented for the AVR to control partial reconfiguration
- Enable Hardware context switching

CacheLogic®

• High-speed, low-power, reconfigurable logic solution

Software Application
Data/Keys
3 DES
RSA
Cache Logic Mode

- Mode designed for CacheLogic applications
  - Device treated as an SRAM by the system
  - Microprocessor treats FPGA as memory mapped I/O.
  - Simple 24 bit Address and 8 bit Data structure.

32 Bit word defines address and data Information for one byte per clock cycle
4 Dimensional Memory Map

- Tag Defines Page being written
- X,Y Define Array Location
- Z defines which byte at a given X,Y Location is written

TAG Addressed PAGES

Cell X Location

Cell Y Location