A Built-In Self-Test Approach for Analog Circuits in Mixed-Signal Systems

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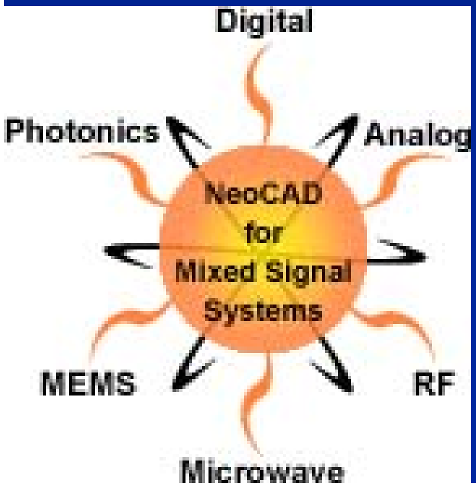


BIST

Auburn University

Built-In Self-Test

Outline of Presentation

- Need for Test & Overview of BIST
- Mixed-Signal BIST Architecture
  - Test Pattern Generator
  - Output Response Analyzer
- Fault Detection with BIST
- Experimental Results
  - Fault Simulation
  - Hardware Prototype
- Parameterized VHDL Model
- Summary & Conclusions
- Demonstration

The Need for Test

2000 International Technology Roadmap for Semiconductors (by the Semiconductor Industry Association - SEMATECH) predicts by 2014:

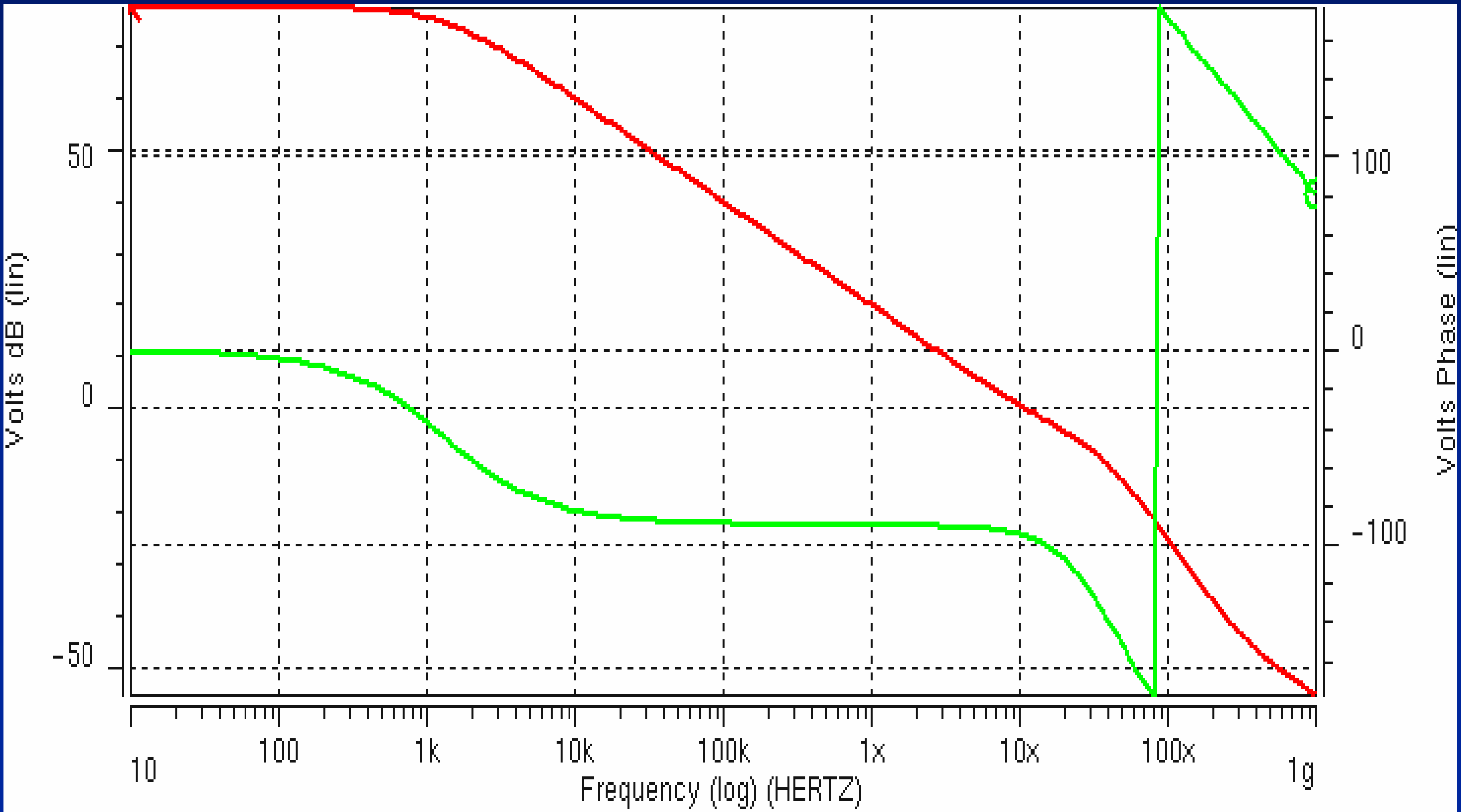
- Test machines will cost ***more than $20M each!!!***
- It will cost ***more*** to test a transistor than to manufacture it!!!
- Built-In Self-Test (BIST) is the most likely solution
  - Analog BIST is needed for mixed-signal systems
  - Fault diagnosis is needed with BIST
  - Methods are needed for automatic implementation of BIST

Analog Circuit Behavior

Frequency response using nominal component values

Gain

Phase

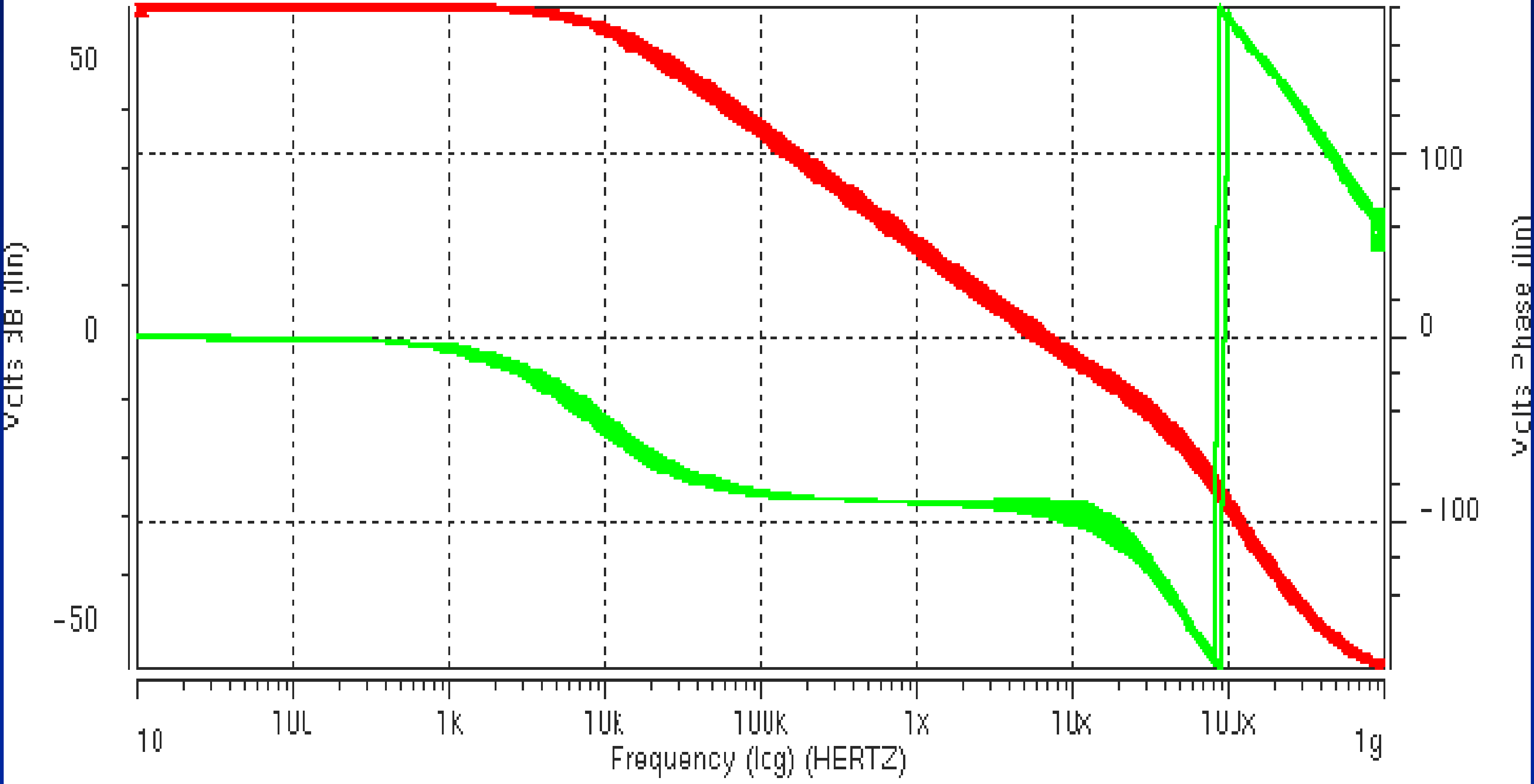


Analog Circuit Behavior

Frequency response using component variations

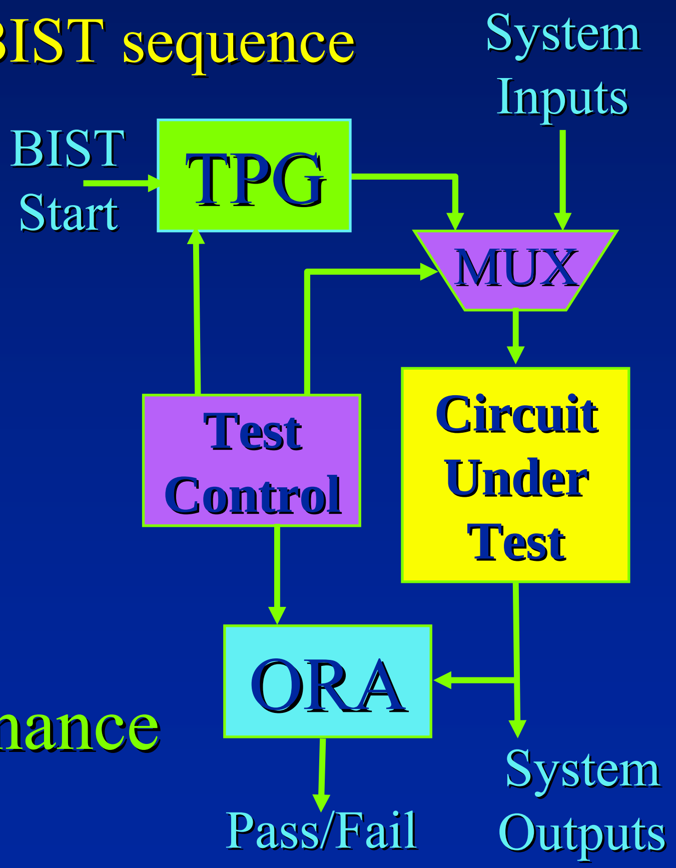
Gain

Phase

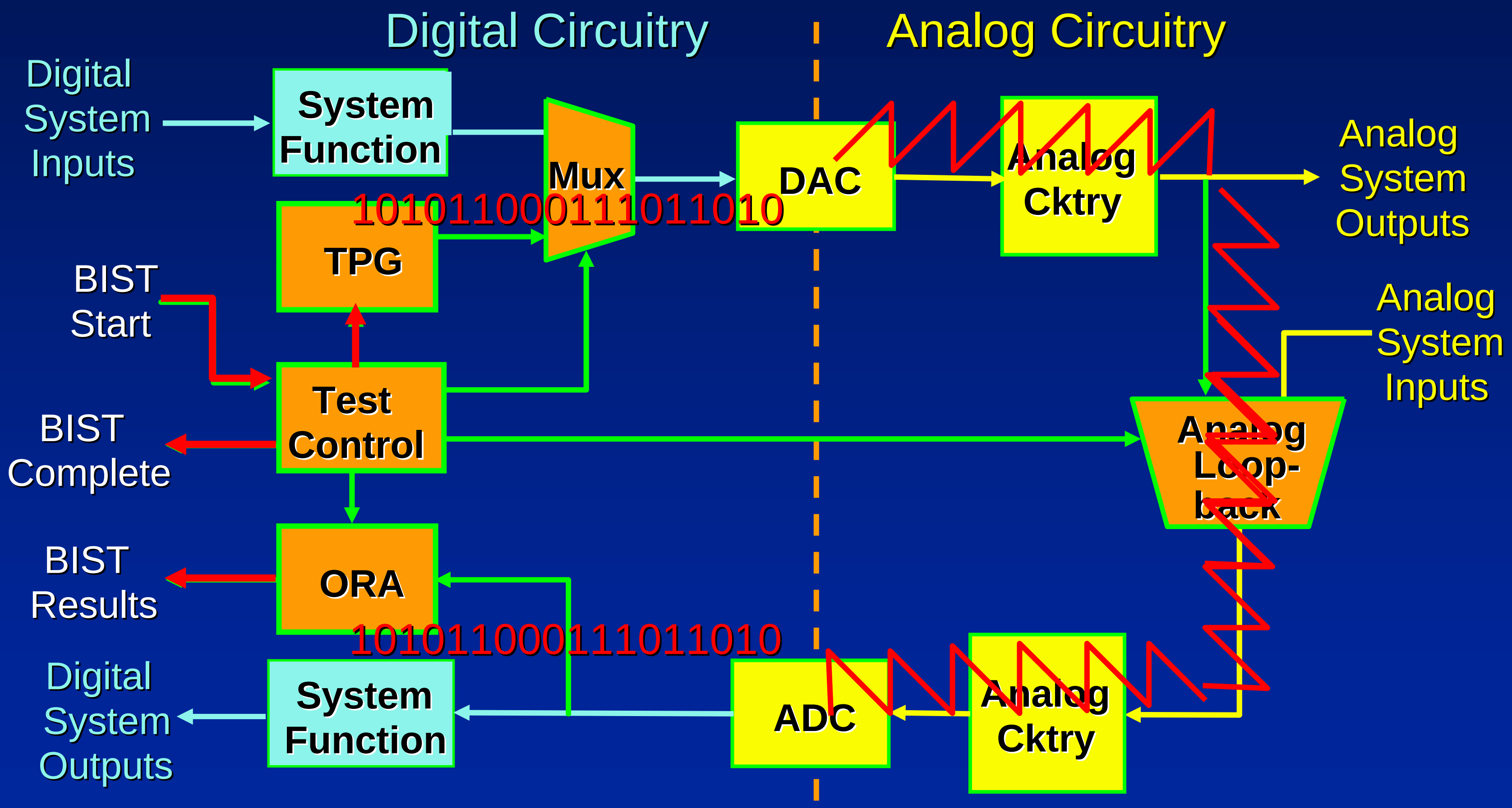


What is Built-In Self-Test?

- ***Basic idea:*** Add circuitry to integrated circuit (chip) or printed circuit board to make it test itself
  - Only power and clock needed during BIST sequence
  - Pass/Fail result reported at end of BIST sequence
    - No need for external test equipment
- Necessary components:
  - Test Pattern Generator (TPG)
  - Output Response Analyzer (ORA)
  - For system level use:
    - Test controller
    - Input isolation
- *Penalties:* area overhead, performance
- *Benefits:* low testing time & cost

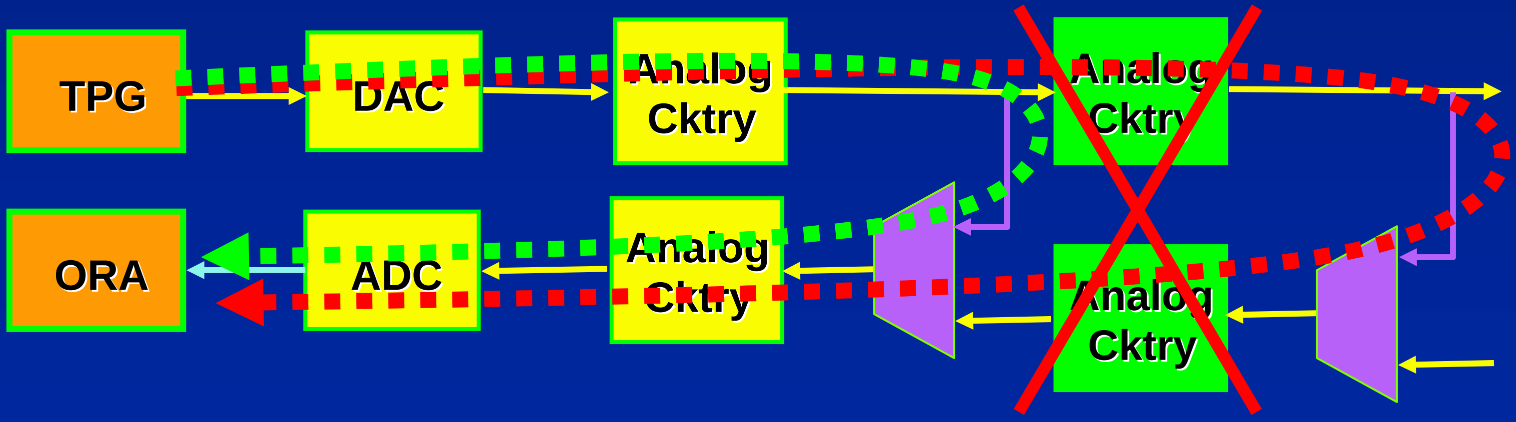


Mixed-Signal BIST Architecture



System-Level Use of BIST

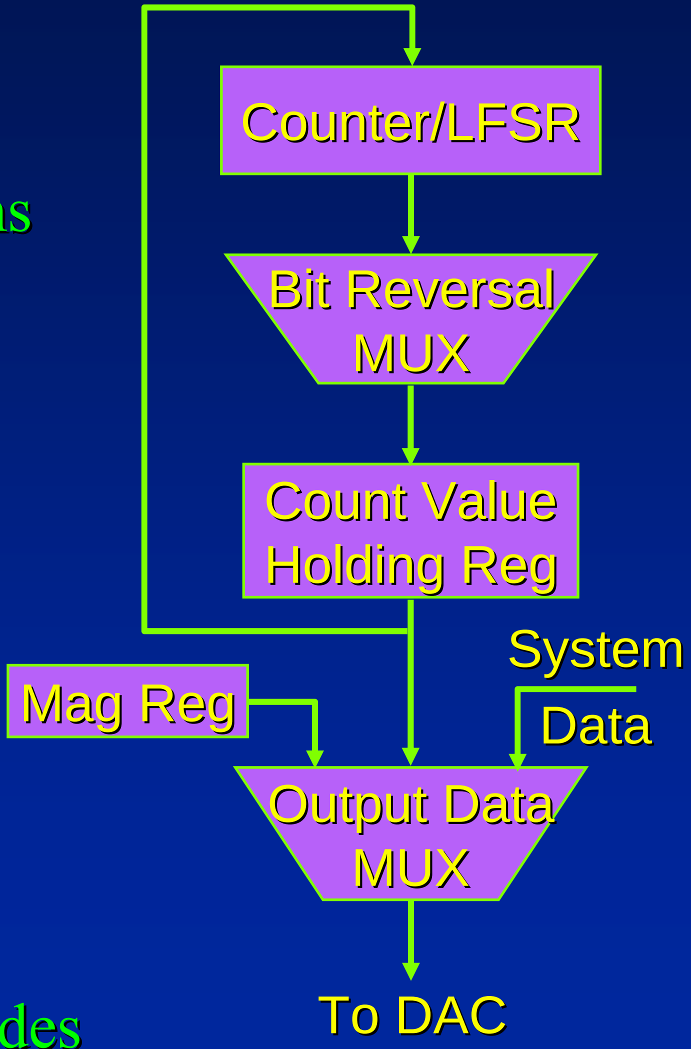
- Multiple BIST sequences w/ analog loopback MUX
  - Pass/fail results indicate location of faulty analog circuitry
- Location & number of analog loopback MUXs
  - Determine analog diagnostic resolution & fault coverage
  - Can trade-off diagnostic resolution and fault coverage with analog area overhead & performance penalties



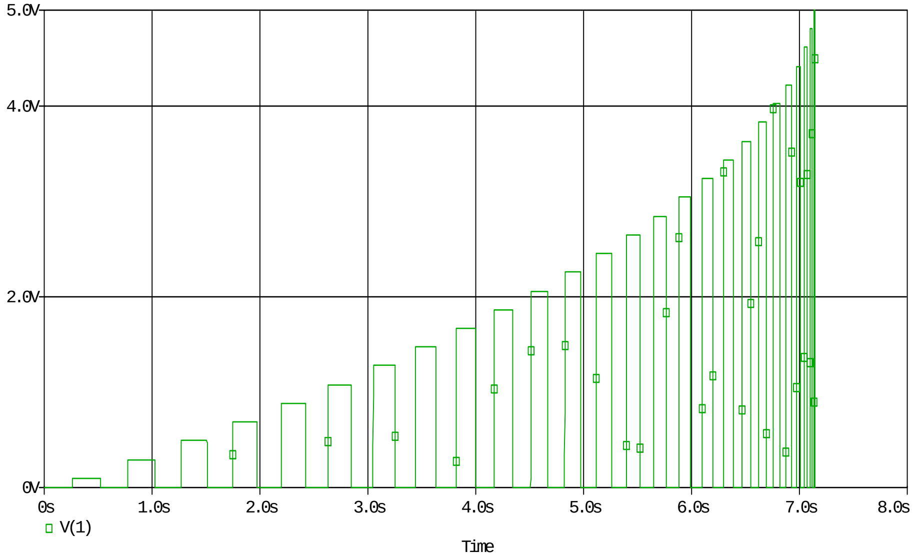
Test Pattern Generation

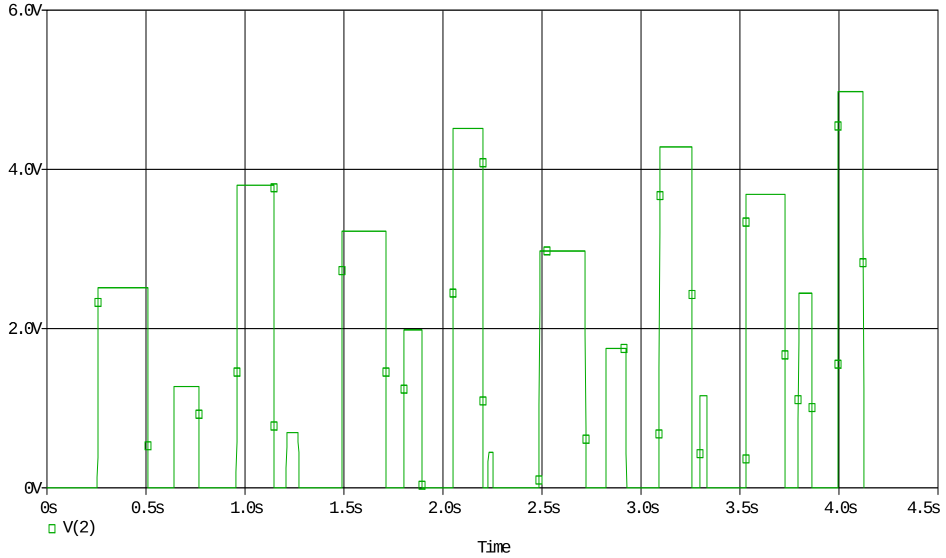
TPG generates 16 test waveforms:

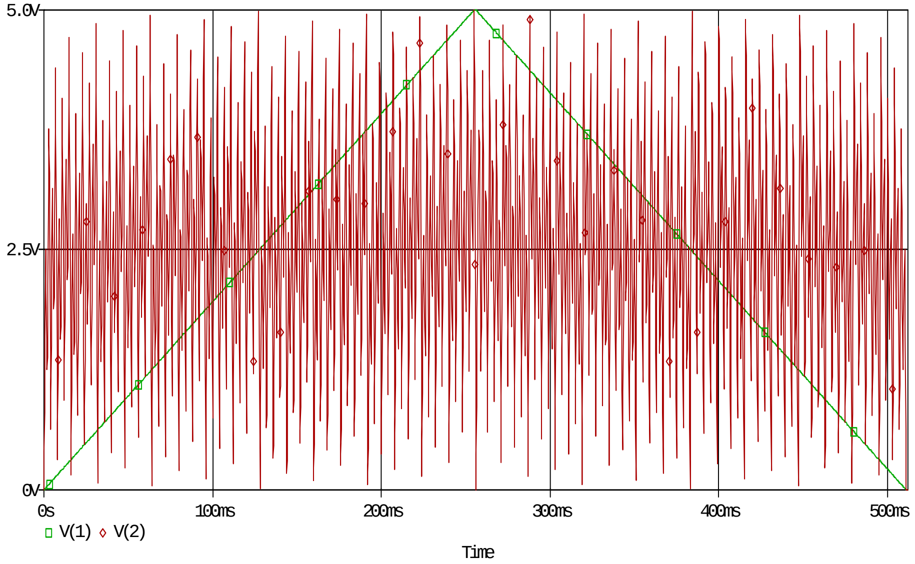
- counter (up, down, & up/down)
  - ramp, sawtooth & triangle waveforms
- LFSR (pseudo-random patterns)
  - noise-like waveforms
- magnitude register
  - programmable amplitude DC test
  - impulse & step responses
- frequency sweep
  - varying & constant amplitudes
- bit reversal (for most waveforms)
  - noise & random frequencies/amplitudes

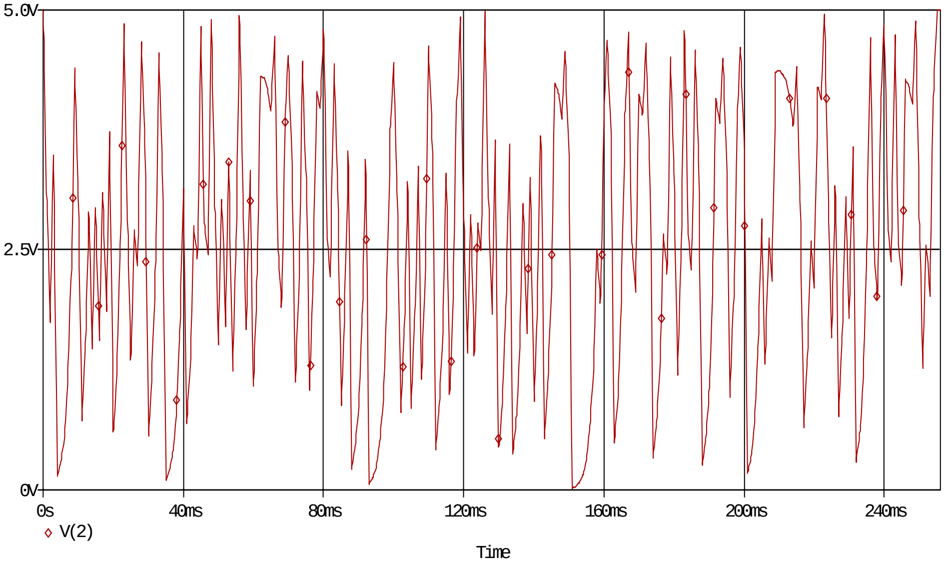


Sample Test Waveforms

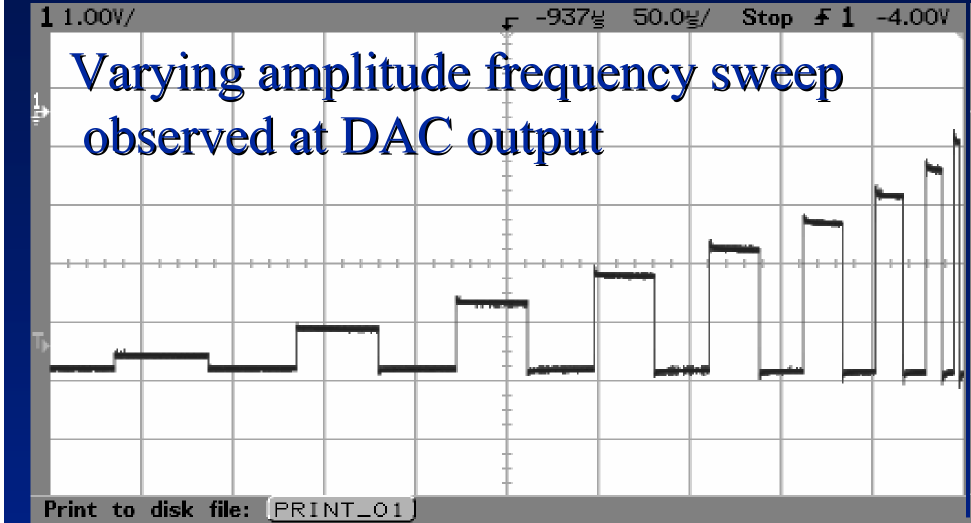


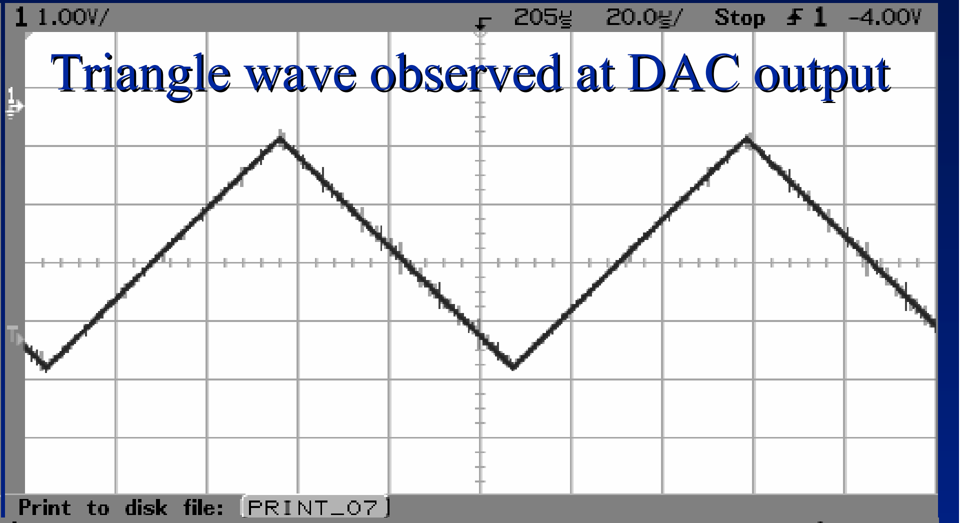


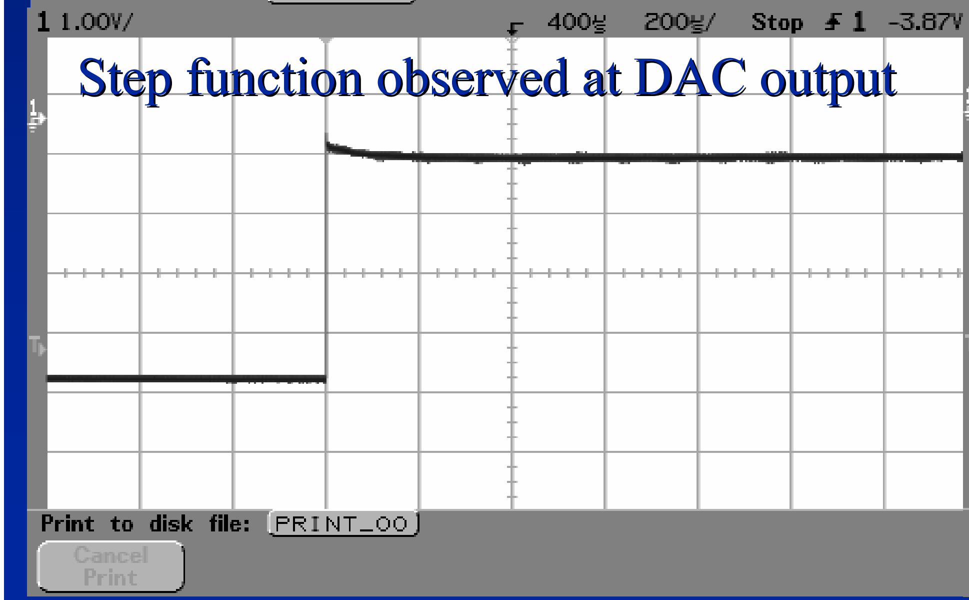


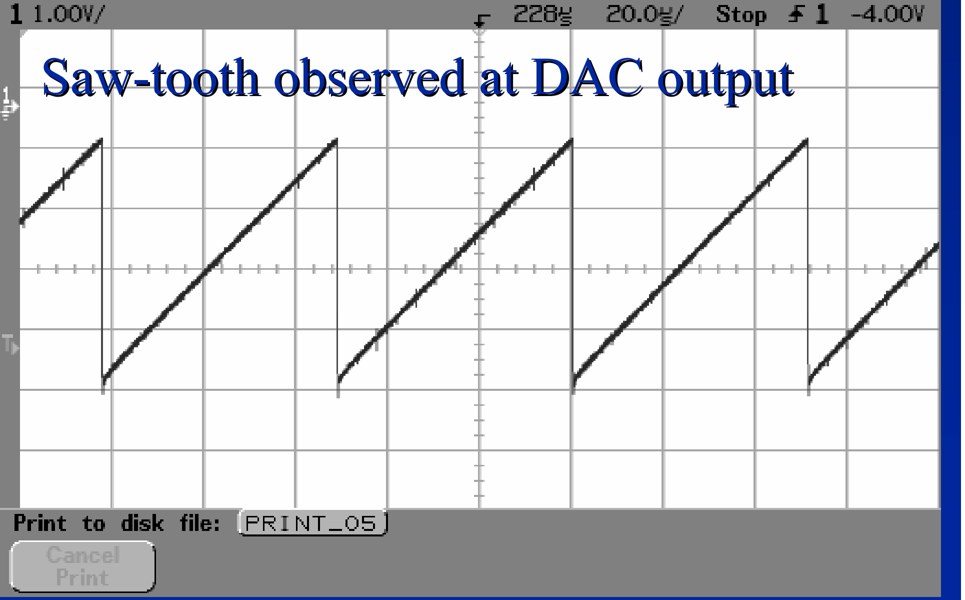


Actual Waveforms from Demo Unit


Varying amplitude frequency sweep observed at DAC output


Triangle wave observed at DAC output

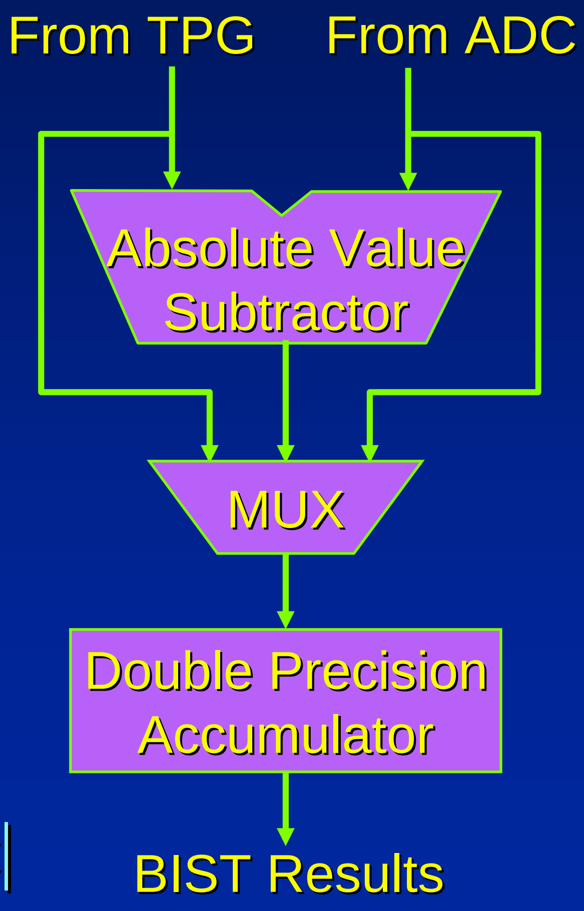

Step function observed at DAC output


Saw-tooth observed at DAC output

Output Response Analyzer

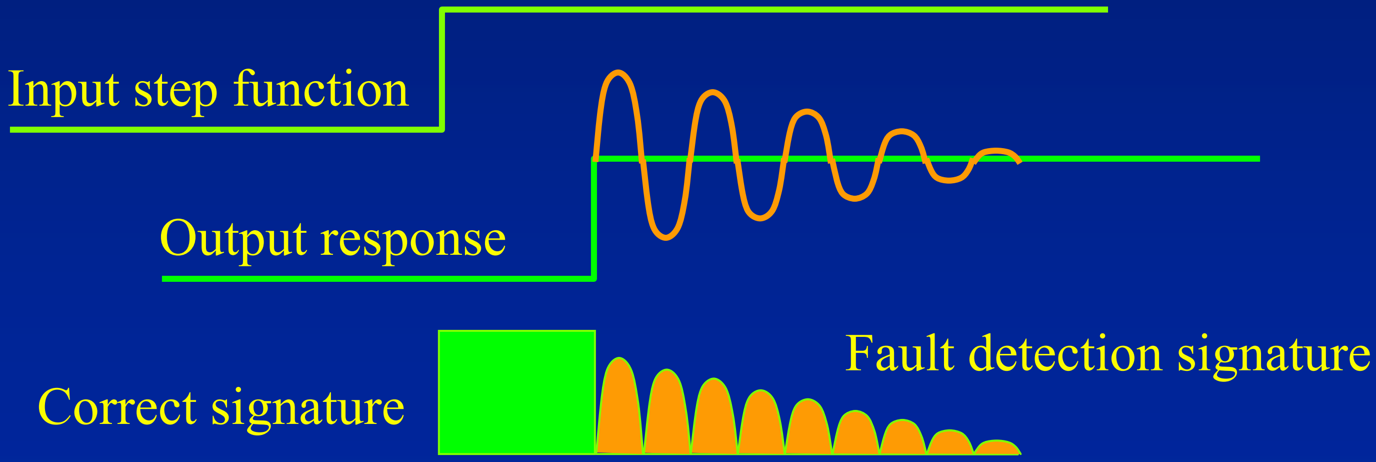
ORA is a double precision accumulator:

- Allows range of values to determine pass/fail status
  - component tolerances
  - processing variation
  - temperature & voltage variation
  - DAC/ADC noise
- Modes of operation:
  - digital test of BIST circuitry
  - analog magnitude test
    - sums ADC output magnitudes
  - analog difference test
    - sums |TPG input - ADC output|



Absolute Value Difference

- Detects faults causing:
  - Noise
  - Phase shift
  - Overshoot/ringing



Input step function

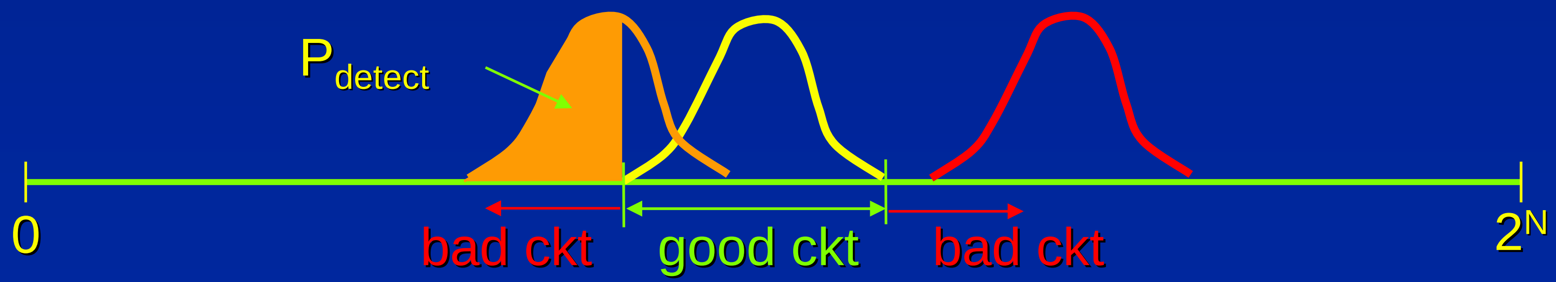
Output response

Correct signature

Fault detection signature

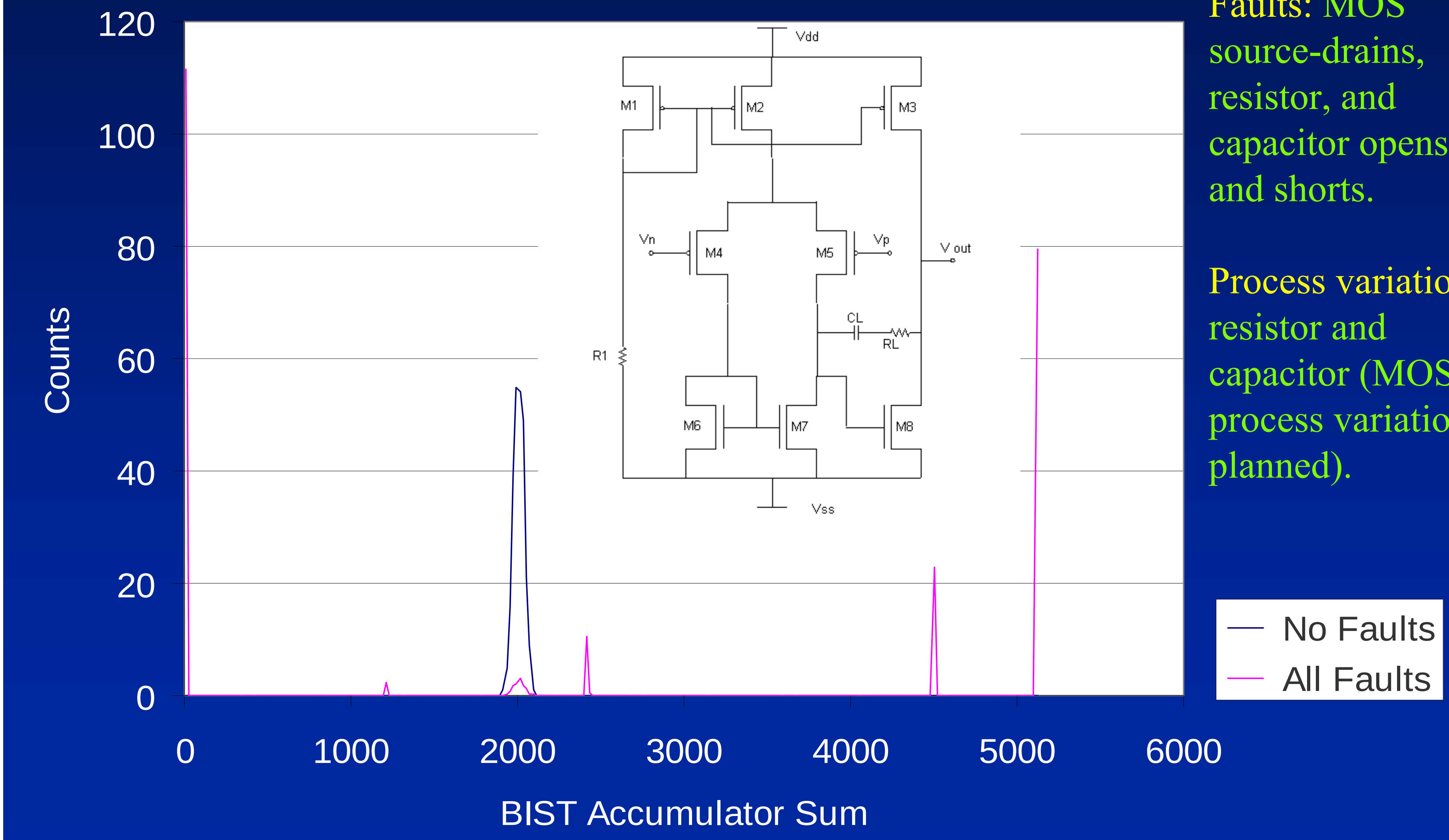
Analog Fault Detection with BIST

- Acceptable variation distributions
  - ***Observation:*** all variations produce normal distribution of signatures
- Detected vs. undetected faults
- Potentially detected faults
  - P_{detect} = #detects/#simulations
- Fault Coverage = (#detect + ΣP_{detect})/#faults



Fault Simulator Results

OpAmp1, Sum Vout, 250 runs, 2/16/02,
-0.1 to 0.1 V sawtooth input, 250-μs period



Faults: MOS source-drains, resistor, and capacitor opens and shorts.

Process variations: resistor and capacitor (MOS process variations planned).

BIST Results with Benchmark Circuits

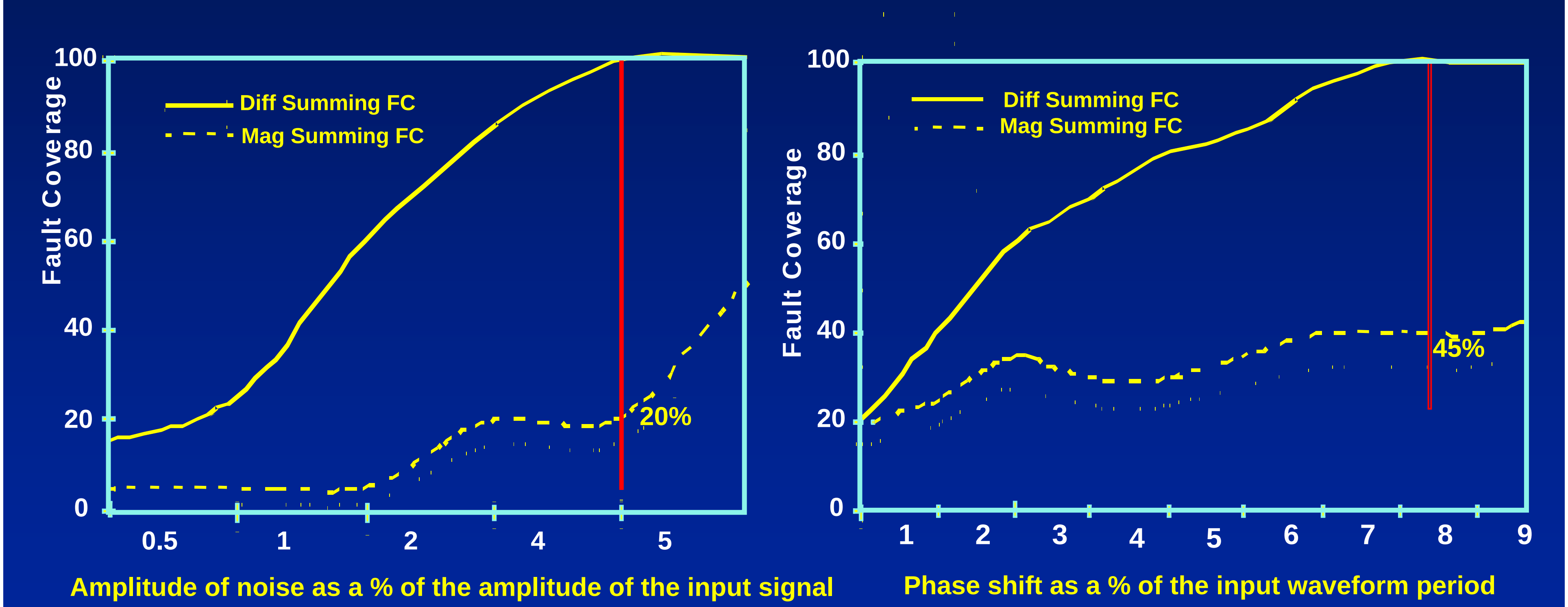
Benchmark Circuit	# Comps	# Op Amps	Hard Faults	Soft Faults	Fault Coverage
Op Amp 1	11	-	22	6	98.6%
CTSV Filter	9	3	84	36	97.8%
Op Amp 2	10	-	20	2	100%
Leapfrog filter	17	6	154	46	100%
Differential amp	9	-	34	18	95.0%
Comparator	3	1	26	8	95.4%
Single stage amp	6	-	16	12	100%
Elliptical filter	22	3	90	62	100%
Low-pass filter	4	1	30	14	100%

General trends:

- Frequency sweep waveforms perform best for filters
- Count/LFSR test waveforms perform best for amplifiers

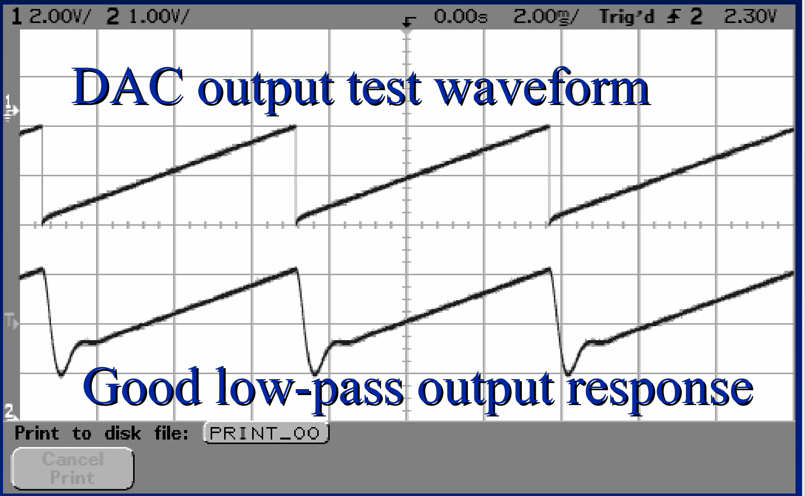
Noise & Phase Shift Detection

Noise and Phase Shift Detection with Difference Summing Mode



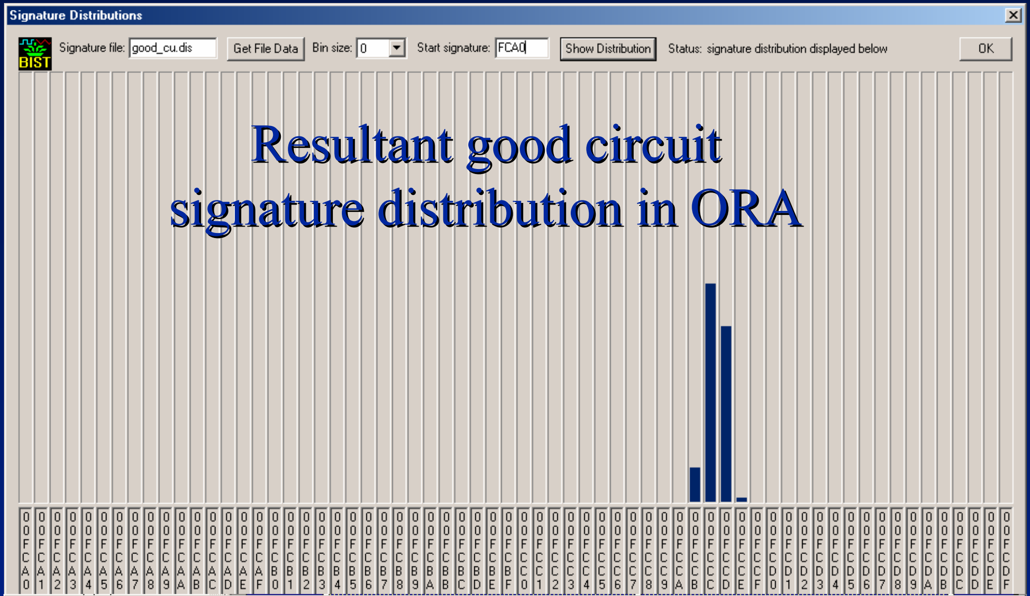
Actual Benchmark Circuit Results

Good low pass filter w/count-up



DAC output test waveform

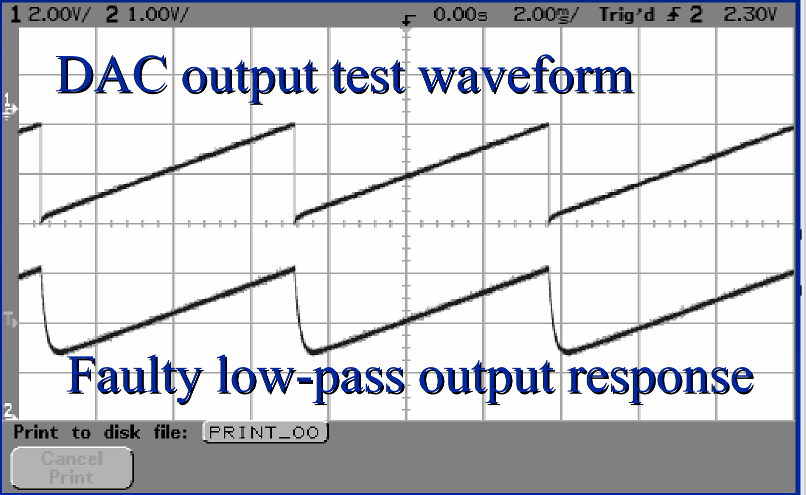
Good low-pass output response



Signature file: good_cu.dis
Bin size: 0
Start signature: FCA0
Status: signature distribution displayed below

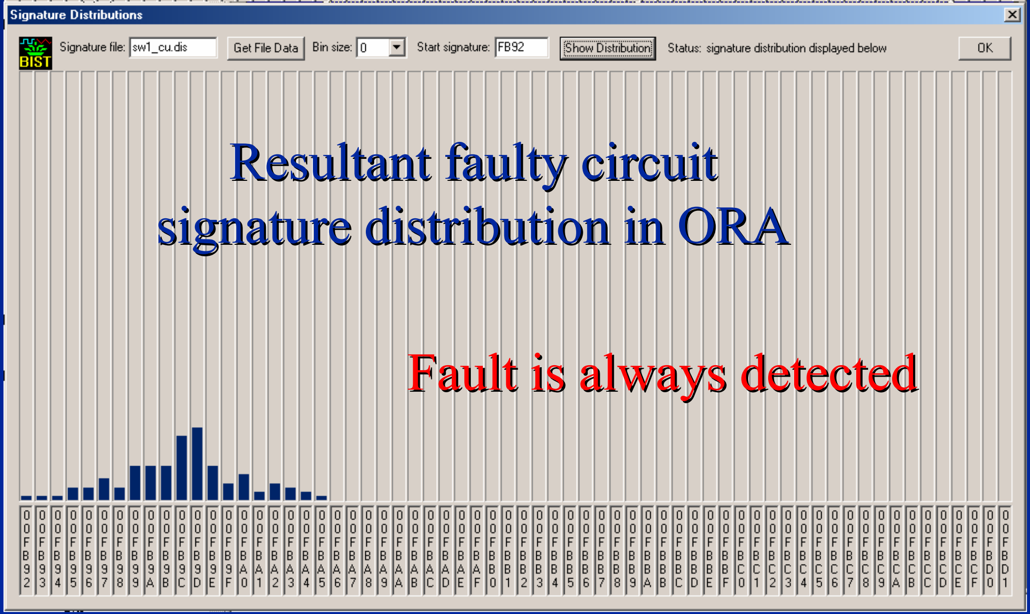
Resultant good circuit signature distribution in ORA

Faulty low pass filter w/count-up



DAC output test waveform

Faulty low-pass output response



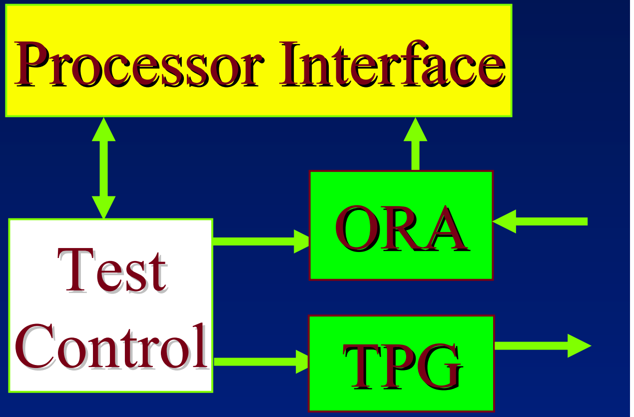
Signature file: sw1_cu.dis
Bin size: 0
Start signature: FB92
Status: signature distribution displayed below

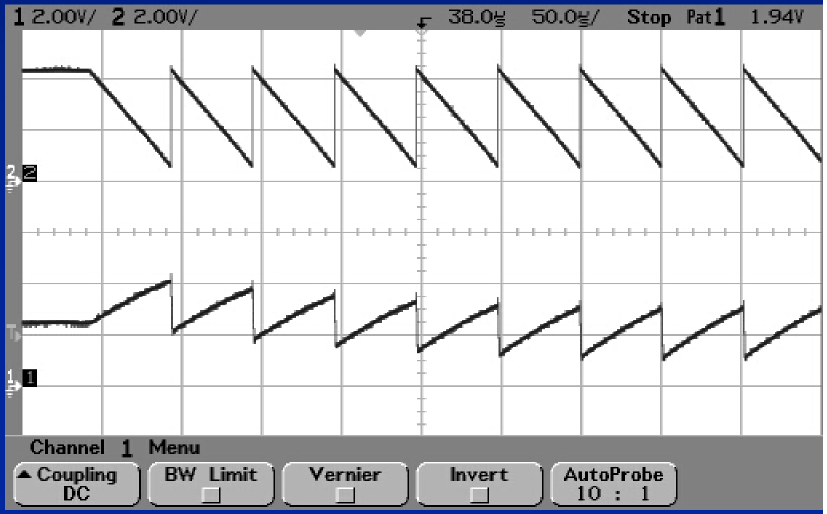
Resultant faulty circuit signature distribution in ORA

Fault is always detected

Parameterized VHDL Models

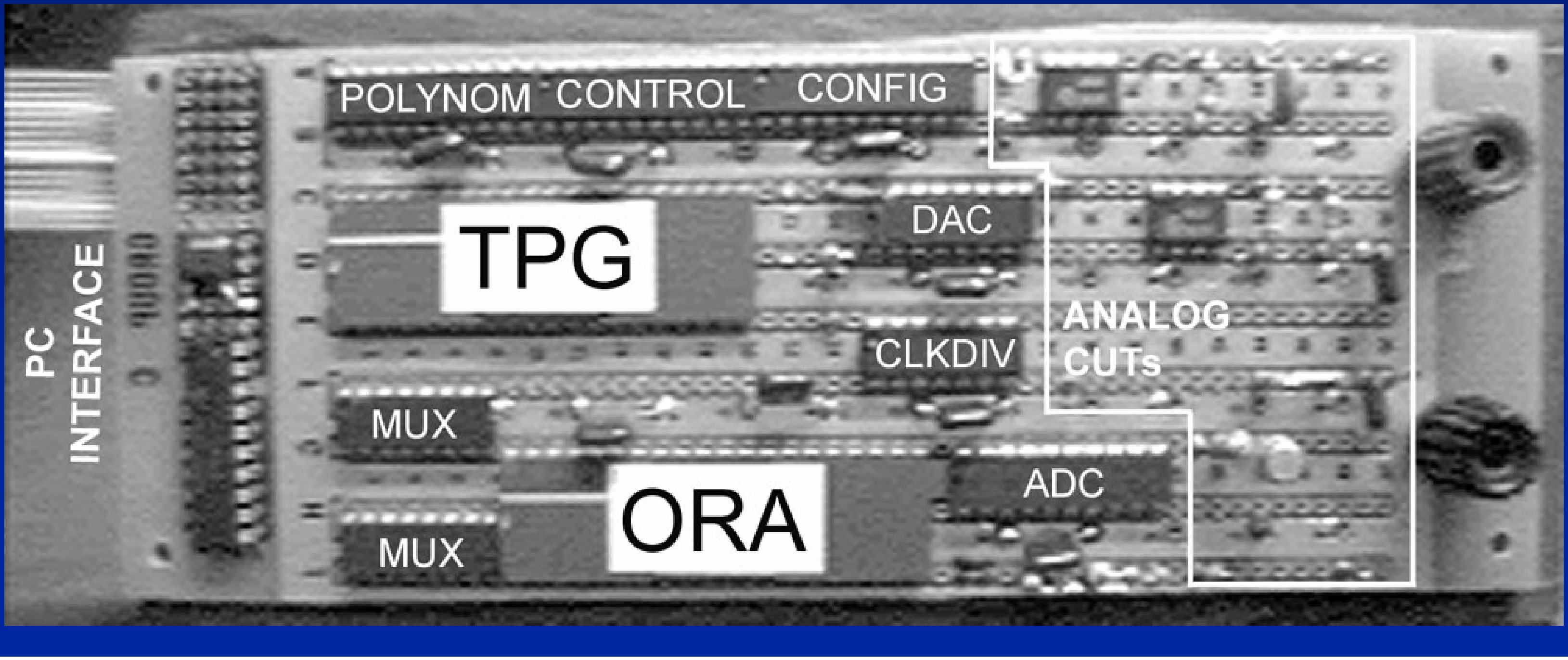
- Automated synthesis in any design
- Parameterized VHDL includes:
  - TPG
    - Supports DAC sizes: 4 to 24-bits
  - ORA
    - Supports ADC sizes: 4 to 24-bits
    - User specified accumulator size
      - Reduces aliasing probability
  - Test controller
    - User programmable initialization & BIST sequence lengths
  - Choice of processor interfaces
    - Custom, serial, parallel
    - IEEE 1149 Boundary Scan



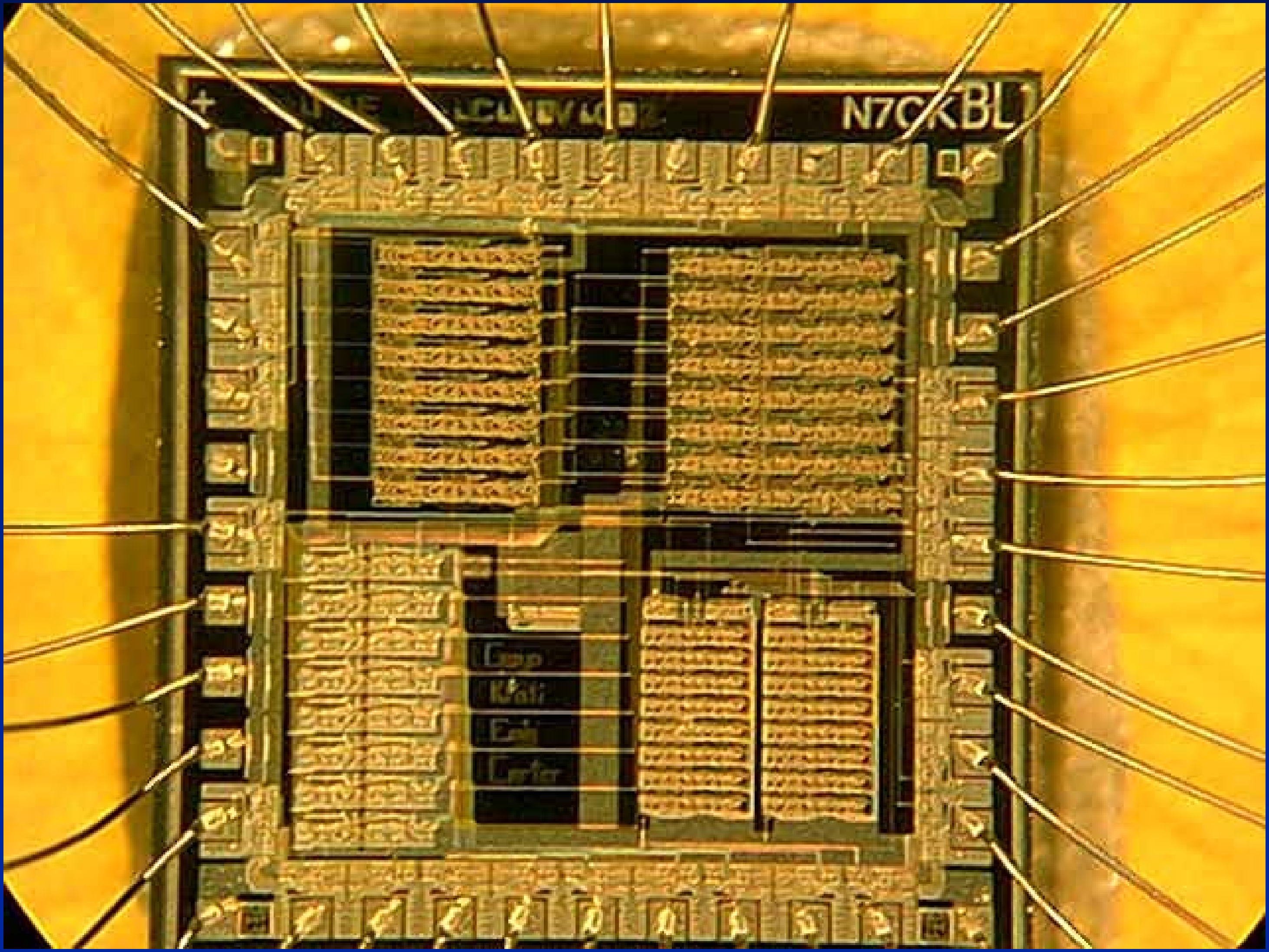


Demonstration Unit 1997

- Original demo unit
  - 3 analog benchmark circuits in discrete parts
    - DAC, OpAmp, & Low Pass Filter

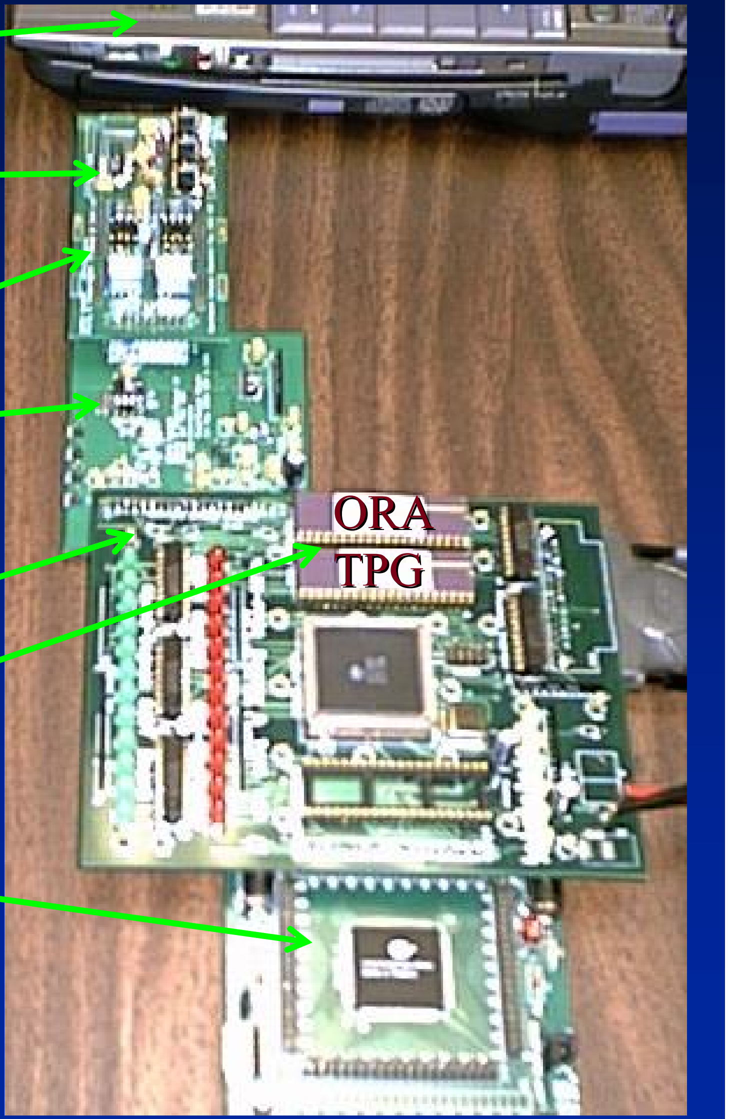


Test Pattern Generator 1997



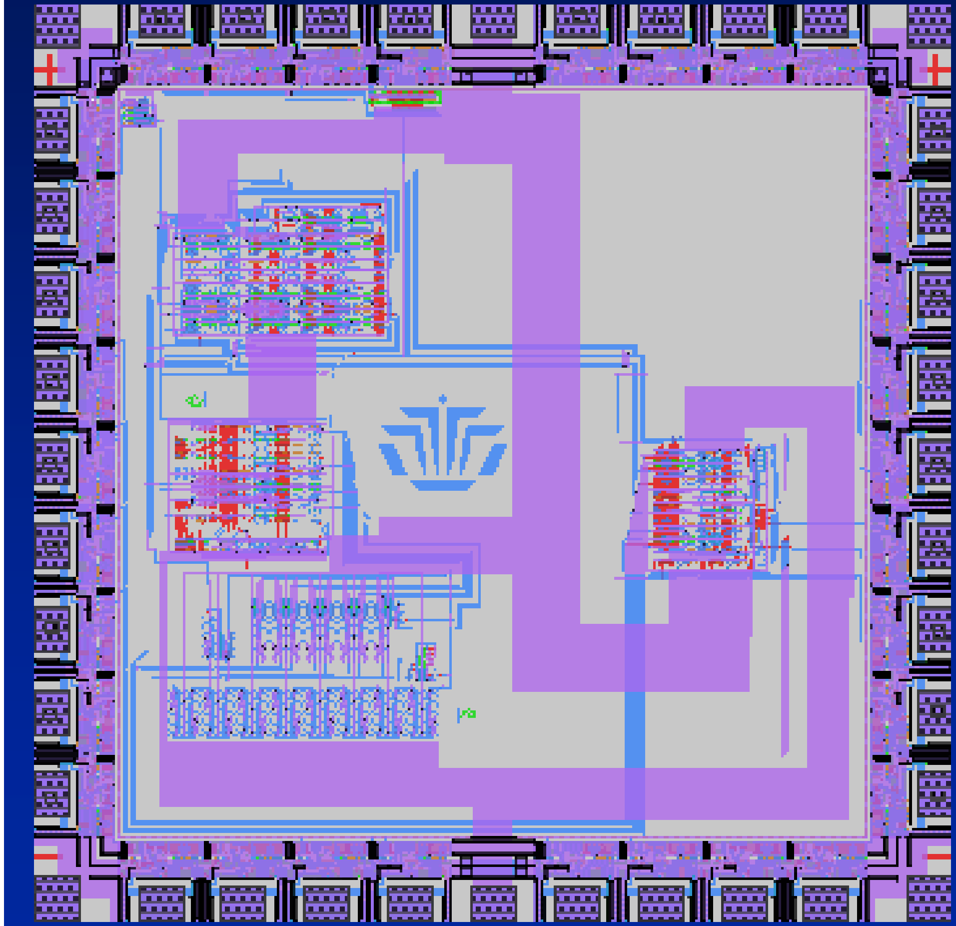
Demonstration Unit 2002

- PC control & display
- Benchmark circuit PCB
  - low/high/band-pass filter
  - with physical fault injection
- DAC-ADC PCB
  - with analog loopback
- Mixed-signal BIST PCB
  - with MOSIS TinyChips
- CPLD-based BIST PCB
  - for synthesis of VHDL
  - parameterized 4 to 12 bits



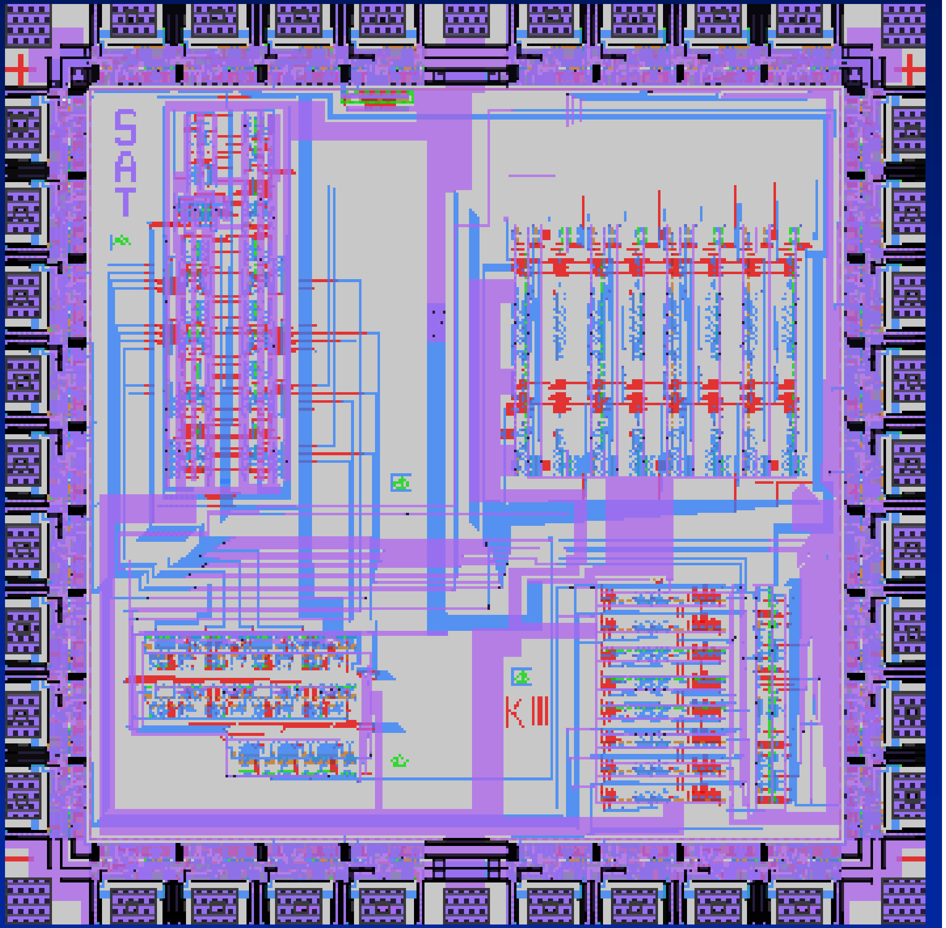
BIST Implementation 2002

Test Pattern Generator



Output Response Analyzer

- Includes test controller

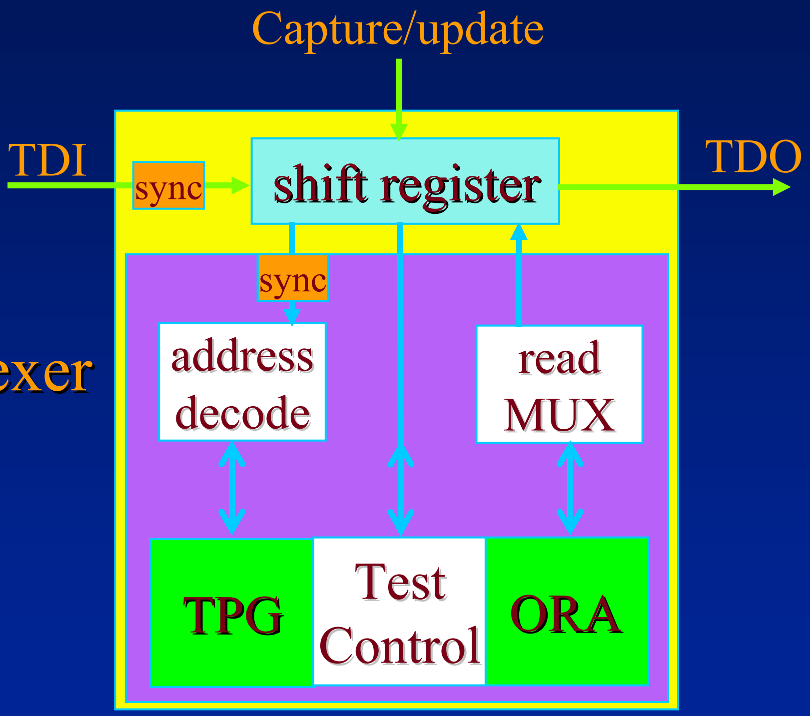


Parameterized VHDL Generics

Generic	Range	Bits controlled by generics
N_{DAC}	$4 \leq N_{DAC} \leq 24$	# inputs to DAC
N_{ADC}	$4 \leq N_{ADC} \leq 24$	# outputs from ADC
N_{ACUM}	$N_{ACUM} \geq \max (N_{ADC,} N_{DAC})$	# bits in 1/2 of double-precision accumulator
N_{PSR}	$N_{PSR} \geq 1$	# bits in freq. sweep shift reg.
N_{ICNT}	$N_{ICNT} + N_{BCNT} \leq N_{ACUM}$	# bits in initialization counter
N_{BCNT}		# bits in BIST counter
N_{LPBK}	$N_{LPBK} \leq N_{ACUM} - 2$	# analog loopback control bits

Processor Interfaces

- Custom Interface
  - incorporation with system specific interfaces
  - all data busses & write enables accessible
- Parallel Interface
  - address decoder & read multiplexer
  - with & without synchronization
- Serial Interface
  - serial shift register
  - with & without synchronization
- Boundary Scan
  - interface to IEEE 1149 standard



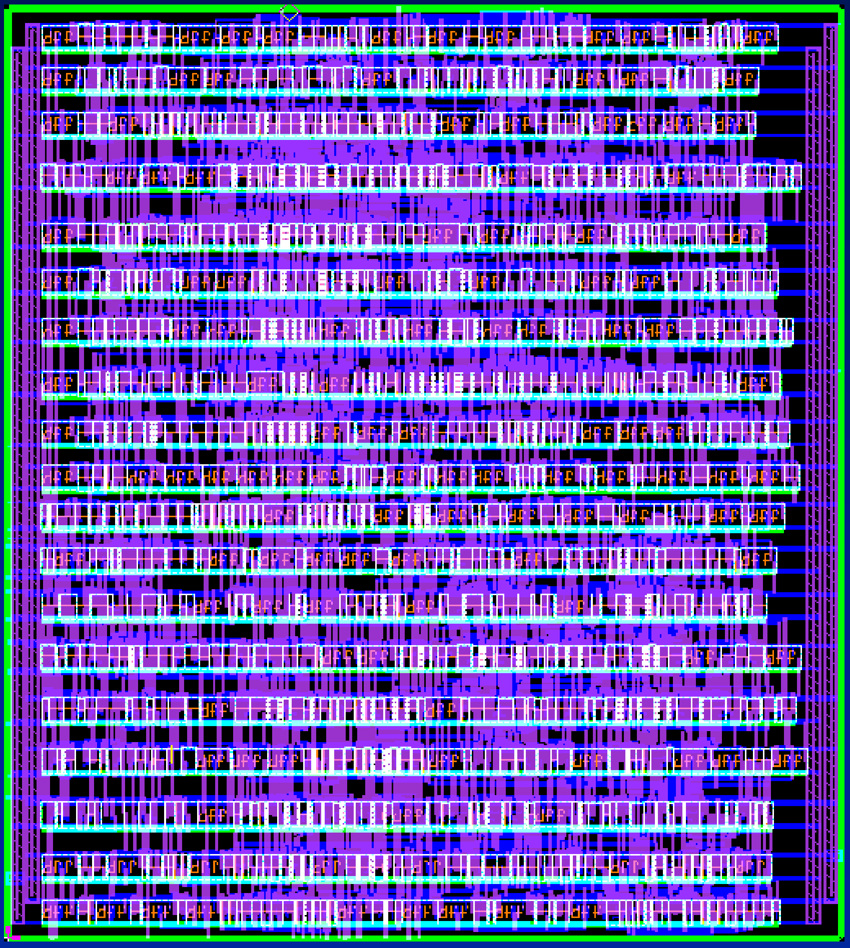
VHDL Synthesis Results

N_{DAC}	N_{ADC}	N_{ACUM}	Area optimize			Speed optimize	
			# gates	**Area** (μm^2)	**Freq.** (MHz)	**#** gates	**Freq.** (MHz)
4	4	12	1044	554961	61.3	1157	94
4	8	12	1100	581594	62.6	1227	89.2
4	12	12	1159	624680	64	1305	86.8
8	4	12	1276	690625	62.6	1441	88.9
12	4	12	1506	801766	64	1716	84.9
12	12	12	1534	809328	64	1773	85.7
8	8	8	1147	599636	91.8	1298	108.7

- AMI 0.5μm CMOS standard cell synthesis results:
  - 745 μm to 900 μm on a side
  - 60 MHz to 109 MHz operation

VHDL Synthesis

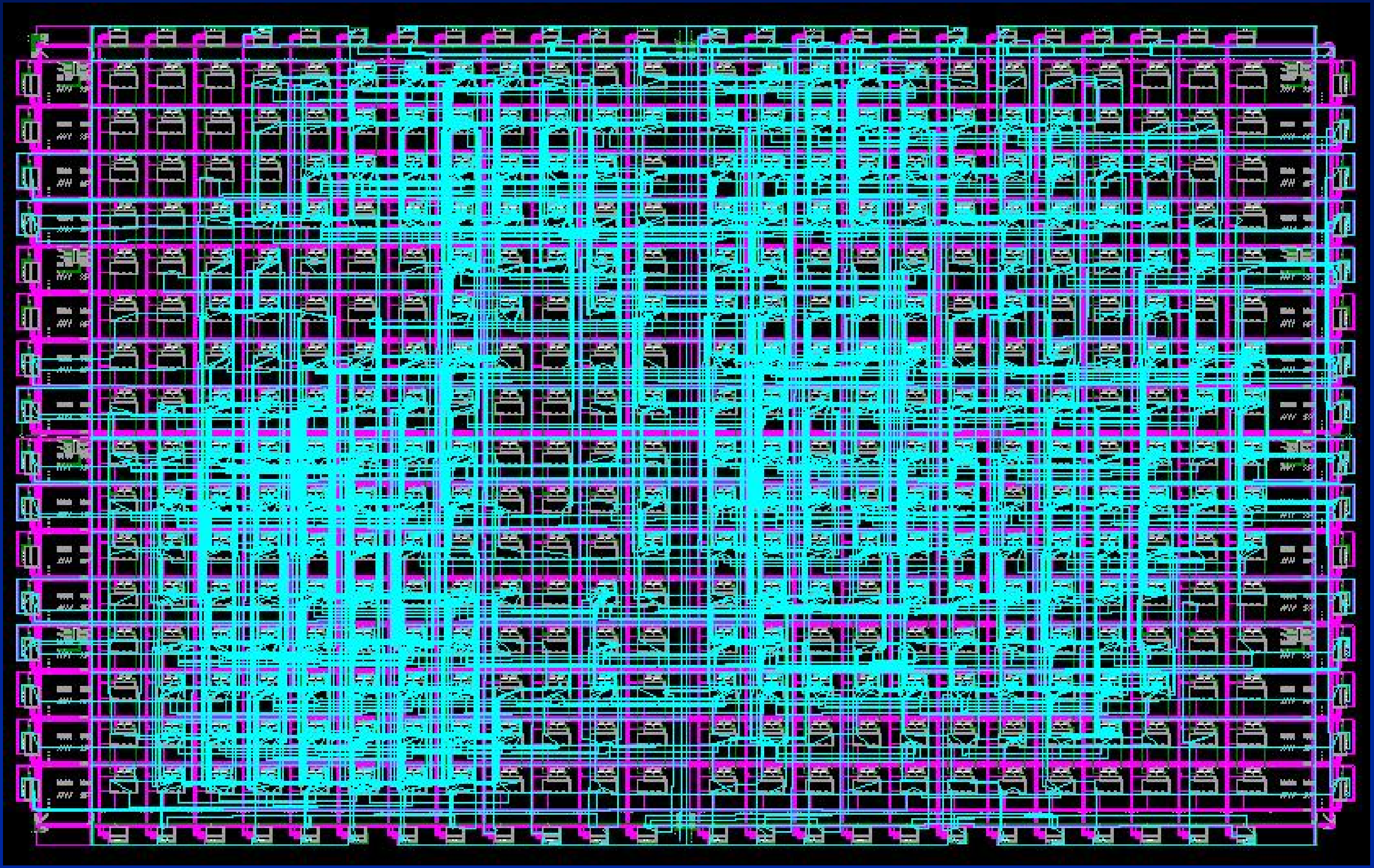
- Used Mentor Graphics
  - serial processor interface
  - 4, 8, and 12-bit versions
- Synthesized & verified
  - via simulation in:
    - 1.5µm AMI CMOS
    - 0.5µm AMI CMOS
  - in actual hardware in:
    - Cypress 39K CPLDs
      - Using WARP
    - Xilinx Virtex FPGAs
      - Using ISE



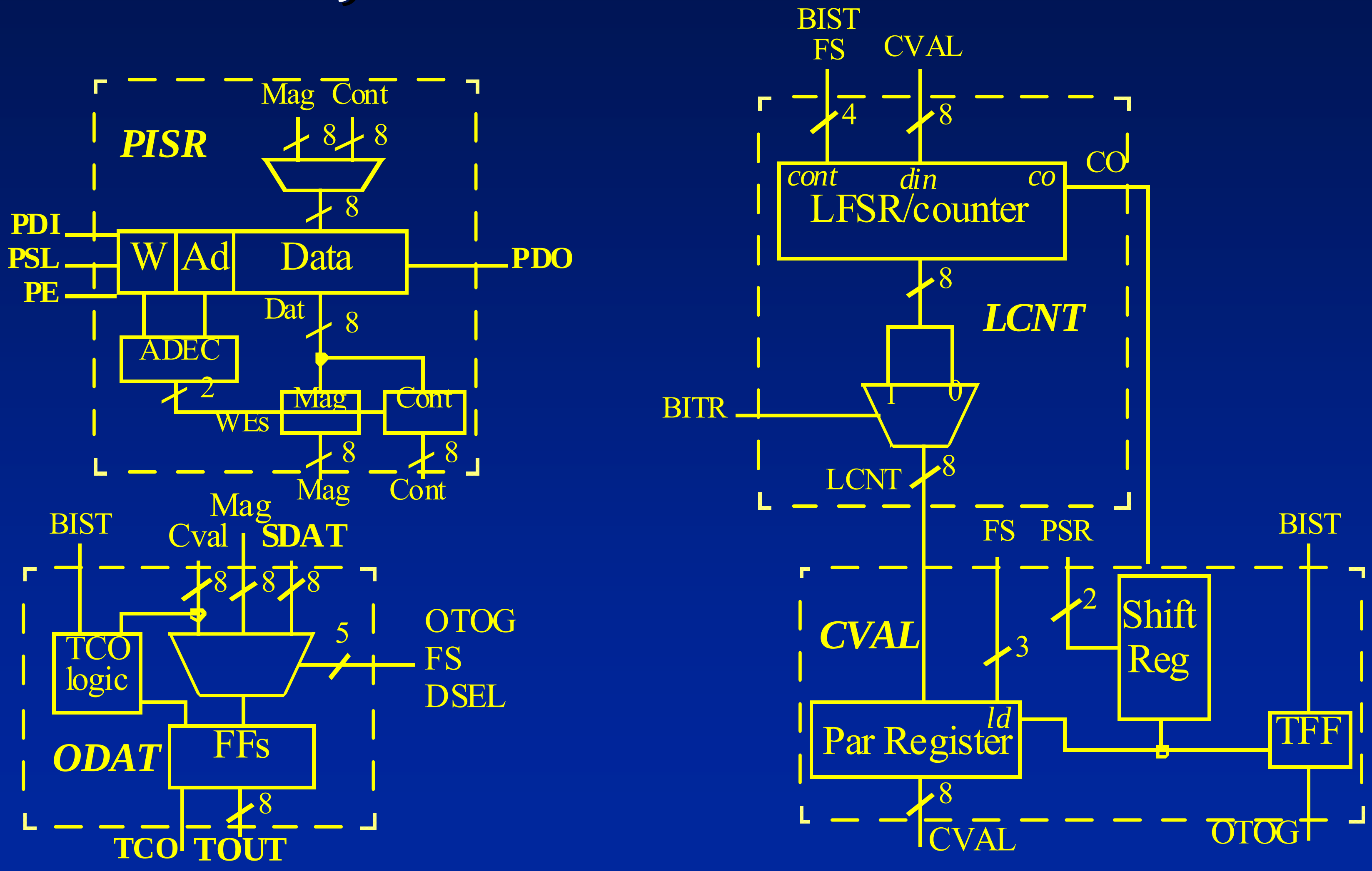
VHDL Synthesis

Synthesis in Spartan 2s50 FPGA

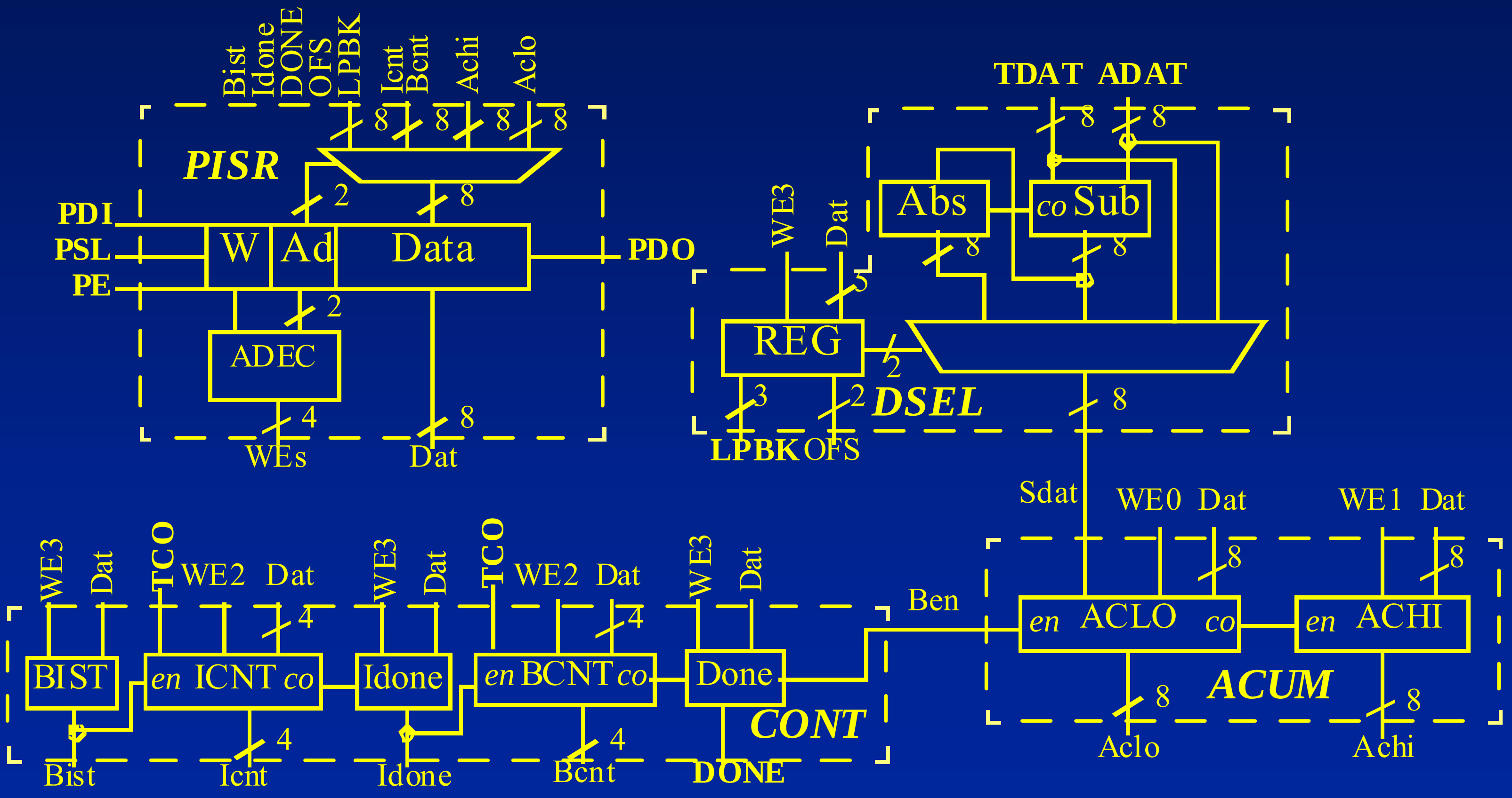
with room to spare



Project TPG Architecture



Project ORA Architecture



Summary & Conclusions

- Most of BIST circuitry in digital domain
  - minimizes impact on analog circuitry
- TPG produces 16 test waveforms
  - high fault coverage in wide variety of analog ckts
- ORA has multiple summing modes
  - accumulator allows range of acceptable values
  - absolute value difference detects noise/phase shifts
- Parameterized VHDL for use in any design
  - implemented & verified in hardware