A Built-In Self-Test Approach for Analog Circuits in Mixed-Signal Systems

Chuck Stroud
Dept. of Electrical & Computer Engineering
Auburn University
Outline of Presentation

- Need for Test & Overview of BIST
- Mixed-Signal BIST Architecture
  - Test Pattern Generator
  - Output Response Analyzer
- Fault Detection with BIST
- Experimental Results
  - Fault Simulation
  - Hardware Prototype
- Parameterized VHDL Model
- Summary & Conclusions
- Demonstration
The Need for Test

2000 International Technology Roadmap for Semiconductors (by the Semiconductor Industry Association - SEMATECH) predicts by 2014:

- Test machines will cost **more than $20M each!!!**
- It will cost **more** to test a transistor than to manufacture it!!!
- **Built-In Self-Test (BIST) is the most likely solution**
  - Analog BIST is needed for mixed-signal systems
  - Fault diagnosis is needed with BIST
  - Methods are needed for automatic implementation of BIST
Analog Circuit Behavior

Frequency response using nominal component values

Gain
Phase

![Graph showing gain and phase response over frequency (log Hertz)]
Analog Circuit Behavior

Frequency response using component variations

Gain

Phase
What is Built-In Self-Test?

- **Basic idea:** Add circuitry to integrated circuit (chip) or printed circuit board to make it test itself
  - Only power and clock needed during BIST sequence
  - Pass/Fail result reported at end of BIST sequence
  - No need for external test equipment
- **Necessary components:**
  - Test Pattern Generator (TPG)
  - Output Response Analyzer (ORA)
  - For system level use:
    - Test controller
    - Input isolation
- **Penalties:** area overhead, performance
- **Benefits:** low testing time & cost
Mixed-Signal BIST Architecture

Digital Circuitry

System Function
TPG
Test Control
ORA
System Function

Analog Circuitry

Mux
DAC
Analog Cktry
Analog Loop-back
ADC
Analog Cktry

Digital System Inputs
BIST Start
BIST Complete
BIST Results
Digital System Outputs

Analog System Outputs
Analog System Inputs
System-Level Use of BIST

- Multiple BIST sequences w/ analog loopback MUX
  - Pass/fail results indicate location of faulty analog circuitry
- Location & number of analog loopback MUXs
  - Determine analog diagnostic resolution & fault coverage
  - Can trade-off diagnostic resolution and fault coverage with analog area overhead & performance penalties
Test Pattern Generation

TPG generates 16 test waveforms:

- **counter (up, down, & up/down)**
  - ramp, sawtooth & triangle waveforms

- **LFSR (pseudo-random patterns)**
  - noise-like waveforms

- **magnitude register**
  - programmable amplitude DC test
  - impulse & step responses

- **frequency sweep**
  - varying & constant amplitudes

- **bit reversal (for most waveforms)**
  - noise & random frequencies/amplitudes
Sample Test Waveforms
Actual Waveforms from Demo Unit

1. **Varying amplitude frequency sweep observed at DAC output**
2. **Triangle wave observed at DAC output**
3. **Step function observed at DAC output**
4. **Saw-tooth observed at DAC output**
Output Response Analyzer

ORA is a double precision accumulator:

- **Allows range of values to determine pass/fail status**
  - component tolerances
  - processing variation
  - temperature & voltage variation
  - DAC/ADC noise

- **Modes of operation:**
  - digital test of BIST circuitry
  - analog magnitude test
    - sums ADC output magnitudes
  - analog difference test
    - sums |TPG input - ADC output|
Absolute Value Difference

- **Detects faults causing:**
  - Noise
  - Phase shift
  - Overshoot/ringing
Analog Fault Detection with BIST

- **Acceptable variation distributions**
  - *Observation:* all variations produce normal distribution of signatures
- **Detected vs. undetected faults**
- **Potentially detected faults**
  - \( P_{\text{detect}} = \frac{\#\text{detects}}{\#\text{simulations}} \)
- **Fault Coverage** = \( \frac{\#\text{detect} + \sum P_{\text{detect}}}{\#\text{faults}} \)
Fault Simulator Results

OpAmp1, Sum Vout, 250 runs, 2/16/02,
-0.1 to 0.1 V sawtooth input, 250-µs period

Faults: MOS source-drains, resistor, and capacitor opens and shorts.

Process variations: resistor and capacitor (MOS process variations planned).
## BIST Results with Benchmark Circuits

<table>
<thead>
<tr>
<th>Benchmark Circuit</th>
<th># Comps</th>
<th># Op Amps</th>
<th>Hard Faults</th>
<th>Soft Faults</th>
<th>Fault Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Op Amp 1</td>
<td>11</td>
<td>-</td>
<td>22</td>
<td>6</td>
<td>98.6%</td>
</tr>
<tr>
<td>CTSV Filter</td>
<td>9</td>
<td>3</td>
<td>84</td>
<td>36</td>
<td>97.8%</td>
</tr>
<tr>
<td>Op Amp 2</td>
<td>10</td>
<td>-</td>
<td>20</td>
<td>2</td>
<td>100%</td>
</tr>
<tr>
<td>Leapfrog filter</td>
<td>17</td>
<td>6</td>
<td>154</td>
<td>46</td>
<td>100%</td>
</tr>
<tr>
<td>Differential amp</td>
<td>9</td>
<td>-</td>
<td>34</td>
<td>18</td>
<td>95.0%</td>
</tr>
<tr>
<td>Comparator</td>
<td>3</td>
<td>1</td>
<td>26</td>
<td>8</td>
<td>95.4%</td>
</tr>
<tr>
<td>Single stage amp</td>
<td>6</td>
<td>-</td>
<td>16</td>
<td>12</td>
<td>100%</td>
</tr>
<tr>
<td>Elliptical filter</td>
<td>22</td>
<td>3</td>
<td>90</td>
<td>62</td>
<td>100%</td>
</tr>
<tr>
<td>Low-pass filter</td>
<td>4</td>
<td>1</td>
<td>30</td>
<td>14</td>
<td>100%</td>
</tr>
</tbody>
</table>

**General trends:**

- Frequency sweep waveforms perform best for filters
- Count/LFSR test waveforms perform best for amplifiers
Noise and Phase Shift Detection with Difference Summing Mode

Amplitude of noise as a % of the amplitude of the input signal

Phase shift as a % of the input waveform period
Actual Benchmark Circuit Results

Good low pass filter w/count-up

DAC output test waveform

Good low-pass output response

Faulty low pass filter w/count-up

DAC output test waveform

Faulty low-pass output response

Resultant good circuit signature distribution in ORA

Fault is always detected
Parameterized VHDL Models

- Automated synthesis in any design
- Parameterized VHDL includes:
  - **TPG**
    - Supports DAC sizes: 4 to 24-bits
  - **ORA**
    - Supports ADC sizes: 4 to 24-bits
    - User specified accumulator size
      - Reduces aliasing probability
  - **Test controller**
    - User programmable initialization & BIST sequence lengths
  - **Choice of processor interfaces**
    - Custom, serial, parallel
    - IEEE 1149 Boundary Scan
Demonstration Unit 1997

- Original demo unit
  - 3 analog benchmark circuits in discrete parts
    - DAC, OpAmp, & Low Pass Filter
Test Pattern Generator 1997
Demonstration Unit 2002

- PC control & display
- Benchmark circuit PCB
  - low/high/band-pass filter
  - with physical fault injection
- DAC-ADC PCB
  - with analog loopback
- Mixed-signal BIST PCB
  - with MOSIS TinyChips
- CPLD-based BIST PCB
  - for synthesis of VHDL
  - parameterized 4 to 12 bits
BIST Implementation 2002

Test Pattern Generator

Output Response Analyzer

- Includes test controller
### Parameterized VHDL Generics

<table>
<thead>
<tr>
<th>Generic</th>
<th>Range</th>
<th>Bits controlled by generics</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_{DAC}$</td>
<td>$4 \leq N_{DAC} \leq 24$</td>
<td># inputs to DAC</td>
</tr>
<tr>
<td>$N_{ADC}$</td>
<td>$4 \leq N_{ADC} \leq 24$</td>
<td># outputs from ADC</td>
</tr>
<tr>
<td>$N_{ACUM}$</td>
<td>$N_{ACUM} \geq \max(N_{ADC}, N_{DAC})$</td>
<td># bits in 1/2 of double-precision accumulator</td>
</tr>
<tr>
<td>$N_{PSR}$</td>
<td>$N_{PSR} \geq 1$</td>
<td># bits in freq. sweep shift reg.</td>
</tr>
<tr>
<td>$N_{ICNT}$</td>
<td>$N_{ICNT} + N_{BCNT} \leq N_{ACUM}$</td>
<td># bits in initialization counter</td>
</tr>
<tr>
<td>$N_{BCNT}$</td>
<td></td>
<td># bits in BIST counter</td>
</tr>
<tr>
<td>$N_{LPBK}$</td>
<td>$N_{LPBK} \leq N_{ACUM} - 2$</td>
<td># analog loopback control bits</td>
</tr>
</tbody>
</table>
Processor Interfaces

- **Custom Interface**
  - incorporation with system specific interfaces
  - all data busses & write enables accessible

- **Parallel Interface**
  - address decoder & read multiplexer
  - with & without synchronization

- **Serial Interface**
  - serial shift register
  - with & without synchronization

- **Boundary Scan**
  - interface to IEEE 1149 standard
VHDL Synthesis Results

<table>
<thead>
<tr>
<th>$N_{DAC}$</th>
<th>$N_{ADC}$</th>
<th>$N_{ACUM}$</th>
<th># gates</th>
<th>Area (µm$^2$)</th>
<th>Freq. (MHz)</th>
<th># gates</th>
<th>Freq. (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>4</td>
<td>12</td>
<td>1044</td>
<td>554961</td>
<td>61.3</td>
<td>1157</td>
<td>94</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>12</td>
<td>1100</td>
<td>581594</td>
<td>62.6</td>
<td>1227</td>
<td>89.2</td>
</tr>
<tr>
<td>4</td>
<td>12</td>
<td>12</td>
<td>1159</td>
<td>624680</td>
<td>64</td>
<td>1305</td>
<td>86.8</td>
</tr>
<tr>
<td>8</td>
<td>4</td>
<td>12</td>
<td>1276</td>
<td>690625</td>
<td>62.6</td>
<td>1441</td>
<td>88.9</td>
</tr>
<tr>
<td>12</td>
<td>4</td>
<td>12</td>
<td>1506</td>
<td>801766</td>
<td>64</td>
<td>1716</td>
<td>84.9</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>12</td>
<td>1534</td>
<td>809328</td>
<td>64</td>
<td>1773</td>
<td>85.7</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>8</td>
<td>1147</td>
<td>599636</td>
<td>91.8</td>
<td>1298</td>
<td>108.7</td>
</tr>
</tbody>
</table>

- AMI 0.5µm CMOS standard cell synthesis results:
  - 745 µm to 900 µm on a side
  - 60 MHz to 109 MHz operation
VHDL Synthesis

- **Used Mentor Graphics**
  - serial processor interface
  - 4, 8, and 12-bit versions
- **Synthesized & verified**
  - via simulation in:
    - 1.5μm AMI CMOS
    - 0.5μm AMI CMOS
  - in actual hardware in:
    - Cypress 39K CPLDs
      - Using WARP
    - Xilinx Virtex FPGAs
      - Using ISE
VHDL Synthesis
Synthesis in Spartan 2s50 FPGA

with room to spare
Project TPG Architecture
Project ORA Architecture
Summary & Conclusions

- Most of BIST circuitry in digital domain
  - minimizes impact on analog circuitry
- TPG produces 16 test waveforms
  - high fault coverage in wide variety of analog ckt's
- ORA has multiple summing modes
  - accumulator allows range of acceptable values
  - absolute value difference detects noise/phase shifts
- Parameterized VHDL for use in any design
  - implemented & verified in hardware