

ELEC 6250 – COMPUTER-AIDED DESIGN OF DIGITAL LOGIC CIRCUITS

[Change to ELEC 5250, Fall 2004]

(Elective for ECPE, Elective for ELEC)

2004 Catalog Data: ELEC 6250. COMPUTER-AIDED DESIGN OF DIGITAL LOGIC CIRCUITS (3) LEC. 3. Pr., ELEC 2220 or COMP 3350. Computer-automated design of digital logic circuits, using discrete gates, programmable logic devices, and standard cells, hardware description languages, circuit simulation for design verification and analysis, fault diagnosis and testing.

Textbook: Application-Specific Integrated Circuits, Michael J. S. Smith., Addison Wesley Longman, Inc., 1997.

References: *VHDL Tutorial & VHDL Design & Simulation with ModelSim EE* Tutorial on line at: <http://www.eng.auburn.edu/department/ee/mgc/mentor.html>

Coordinator: Charles E. Stroud, Professor of Electrical & Computer Engineering

Course Objectives:

1. To be able to use computer-aided design tools for development of complex digital logic circuits
2. To be able to model, simulate, verify, analyze, and synthesize with hardware description languages
3. To be able to design and prototype with programmable logic

Prerequisites by topic:

1. Digital logic design and analysis or switching theory
2. Computer system organization and design

Topics:

Class schedule (50 minute classes):

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| 1. Hierarchical design concepts and technologies for digital circuits | (2 classes) |
| 2. Low-level design and modeling of digital circuits | (3 classes) |
| 3. CAD tools for schematic capture, logic simulation, and timing analysis | (4 classes) |
| 4. Synchronous and asynchronous sequential circuit design methods | (4 classes) |
| 5. Hierarchical design methods | (2 classes) |
| 6. Modeling and automatic synthesis of digital circuits using VHDL | (8 classes) |
| 7. Design with CPLDs and FPGAs | (6 classes) |
| 8. Design with standard cells | (2 classes) |
| 9. Fault modeling and fault simulation | (6 classes) |
| 10. Digital logic testing and design for testability | (3 classes) |
| 11. Tests and project reviews | (4 classes) |

Typical methods for evaluating student performance:

Hour quizzes (2)	50%
Final exam	25%
Design projects	25%

Design Project:

A specification-oriented design project will be an integral part of the course which will include modeling, simulation, and synthesis of VHDL into standard cells and field programmable gate arrays. The design project will change each semester and will include development of test vectors and fault simulation analysis of the test vectors and design. Note that every student is expected to do his/her own project. Discussion of various aspects of the project with fellow students is acceptable, provided that designs are not copied.

Class attendance: Class attendance is encouraged, but will not be accounted for in the course grade.

Policy on unannounced quizzes: There will be no unannounced quizzes.

Special Accommodations: Any student requiring special accommodations should come by the instructor's office within the first two days of class, bringing your letter from the Office of Students with Disabilities.

Contribution of course to meeting the professional component

Engineering topics: 3 credits

33% engineering science (1 credit)

67% engineering design (2 credits)

Primary program outcomes related to this course:

Outcome 1. Ability to apply knowledge of math, science and engineering to solve problems.

Outcome 2. Ability to apply in-depth knowledge in one or more disciplines

Outcome 3. Ability to design an electrical component or system to meet desired needs.

Outcome 6. Proficiency in the use of computers and other modern tools to solve engineering problems.

Prepared by: C. E. Stroud

Date: February 20, 2004