Hierarchical & Parameterized VHDL Modeling, Simulation, & Synthesis

ELEC 4200

Auburn University

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Overview

• Write a parametrized VHDL model for a rising edge-triggered N-bit universal register/counter with following specifications (in order of precedence):
  • Active high reset (RST)
  • Active high clock enable (CE)
  • Two mode control inputs (M1 & M0)
• See function table for modes of operation
• Simulate & verify design for at least 2 different values of \( N \)
• Synthesize, download & verify multiple implementations of design in Spartan 3 FPGA
• Note: during shift register mode \( Q_{n-1} \leftarrow D_{n-1} \)

<table>
<thead>
<tr>
<th>RST</th>
<th>CE</th>
<th>M1</th>
<th>M0</th>
<th>Q^+</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>( Q_1^+ \leq 0 )</td>
<td>Reset</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>( Q^+ \leq Q )</td>
<td>Hold</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>( Q_1^+ \leq Q_{i+1} )</td>
<td>Shift</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>( Q^+ \leq Q+1 )</td>
<td>Count</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>( Q^+ \leq \text{Din} )</td>
<td>Load</td>
</tr>
</tbody>
</table>
1. Write a parameterized VHDL for the register/counter using the specifications on the previous page
2. Write a separate VHDL model for the digital one-shot from Lab 4
3. Write a hierarchical VHDL model that calls and connects the register/counter model and the digital one-shot mode
   - Where the output of the digital one-shot drives the clock enable (CE)
4. Determine the values of $N$ you will use for simulation and design verification
5. Determine the FPGA pin numbers you will use for LEDs, push buttons, and/or switches during operation in the FPGA for the various values of $N$
   - Make a table of these pin numbers and their functions
1. Do the following for a value of N
   • Simulate and verify your register/counter VHDL
   • Simulate and verify your hierarchical model that calls the register/counter and the digital one-shot
   • Synthesize your design for the Spartan3 using your input and output pin assignments
     • Record the number of flip-flops (FFs), LUTs, and slices used
     • Test your circuit using the PCB LEDs, switches, and/or push buttons
   • Demonstrate your working decoder to the GTA

2. Repeat Step 1 for another value of N
Create one of the following circuits:

1. Counter (tie M1=1 and M0=0)
2. Shift register (tie M1=0 and M0=1)
3. Parallel load register (tie M1=1 and M0=1)

IMPORTANT
RST and CE must still be functional on your circuits

4. Demonstrate your working circuit to the GTA
5. Record the number of flip-flops (FFs), LUTs, and slices used
6. Repeat steps 4 and 5 for the other two circuits
What values did you choose for N and why?
What would be the advantages of choosing the values of 6 & 8 for N when simulating the circuit.

Report Guidelines

1. Verified parameterized VHDL models
2. Screenshot of your ModelSim simulation results
3. Table of synthesis results for each of the 5 circuits
   - First value of N
   - Second value of N
   - Counter
   - Shift Register
   - Parallel Load Register
4. All pre-lab work, including FPGA pin numbers
5. Answers to questions