Simulation and Synthesis of a Stored Program Computer Architecture

ELEC 4200

Auburn University

November 7th, 2010
• Write a VHDL model for the input interface to connect the Boundary Scan port and Shift Register from Lab 8 to PicoBlaze
• Write a hierarchical model to interconnect the following:
  • PicoBlaze with assembled program memory that meets the specifications on the next page
  • Boundary Scan port interface circuitry to PicoBlaze
• Simulate, debug, and verify the operation of your design
• Download, debug, and verify the operation of your PicoBlaze architecture and program on the Spartan 3 FPGA
• Interface circuitry for Boundary Scan to PicoBlaze
  • 6-bit shift register as in Lab 8
  • Another level sensitive 6-bit latch enabled by BSCAN
    Update may be used to hold address and data passed to PicoBlaze

• Interface circuitry for PicoBlaze to 7-segment display
  • 11-bit register enabled by PicoBlaze WRITE_STROBE is useful to hold 7-segment values plus the display enables
  • Note: only one display enable should be active at a time

• PicoBlaze functional specifications
  • Takes 4-bit HEX data and 2-bit address from BSCAN interface and stores it in 1 of 4 registers depending on 2-bit address
  • Note: data for each of the 4 displays can be updated anytime via BSCAN
  • Decodes HEX data to 7-segment display data
  • Passes 7-segment data to display using port ID to enable digit sequence to continuously display 4 independent values
• **Advanced Design**
  - In addition to regular system specifications, PicoBlaze displays “ELEC” then “4200” before displaying the 4 BS written 7-segment display values for 4 seconds, then the sequence repeats

• **Super Design**
  - “ELEC 4200” scrolls across display between displaying the 4 BS written 7-segment display values for 4 seconds
1. Study PicoBlaze architecture and instruction set
   - Write your PicoBlaze program
   - Note: the brightness of the display of the individual 4 hex digits is a function of how often and how long a given 7-segment display is being driven by the processor, which must be managed in the program

2. Write VHDL models for
   - BS to PicoBlaze interface circuitry
   - PicoBlaze to 7-segment display interface circuitry
   - Top level model to interconnect PicoBlaze and other models
1. Simulate and debug your PicoBlaze program via pBlazeIDE
2. Assemble your verified program via KCPSM3.exe
3. If possible, simulate and verify your top level VHDL model interconnecting all components
4. Synthesize, download, and verify your complete design
5. Demonstrate your complete design to GTA
Final Lab Report

Report must contain

1. A description of the design you chose (regular, advanced, super) and why
2. A description of the various levels of simulation, synthesis, and download to the FPGA you did and why
3. A discussion of what went right and wrong in your approach to design and design verification
4. A discussion of what you would have done differently if you were starting over with this particular project
5. Your VHDL models and PicoBlaze program(s) should be included in this report and referred to in your discussion
6. There is no need to turn in your code separately