Combinational Design Using Schematic Capture

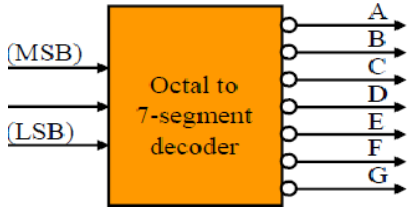
ELEC 4200

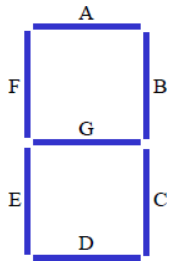
Auburn University

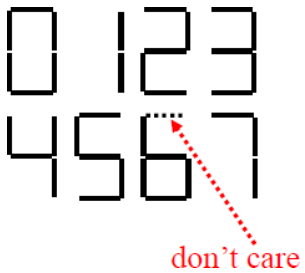
August 29^{th}, 2011

Overview

- Design an octal to 7-segment decoder with active-low outputs
  - Inputs D2-D0
  - Outputs A-G
- Generate:
  - Complete truth table
  - K-maps
  - Minimized SOP equations
  - Logic diagram
- Capture schematic using SOP equations, simulate, and verify design (debugging where needed) using ModelSim
- Synthesize using ISE, download, and verify design onto a Spartan 3 FPGA







Pre-lab Assignment

1. Derive the truth table for the decoder
2. Use K-maps to obtain minimized SOP expressions
   - Share common product terms and gates where possible
3. Draw a logic diagram
   - Share common product terms and gates where possible
   - Label all inputs and outputs according to the system specifications
4. Read the following:
   - ISE Quick Start Guide (pages 24-30)
   - Spartan 3 PCB reference manual
     - Chapter 1 (4 pages)
     - Chapter 3 (3 pages)
     - Chapter 4 (2 pages)

Lab Exercise

1. Capture your design using the ISE Schematic capture tool
2. Simulate your circuit for design verification
   - Simulate & verify all possible input values
   - Debug & fix problems if output is incorrect
     - Check truth table against K-map population
     - Check K-map groups against logic equation product terms
     - Check logic equations against VHDL model equations

Lab Exercise (continued)

3. Synthesize your design for the Spartan3 S200 FPGA using ISE
   - Connect inputs (D2-D0) to switches
   - Connect outputs (A-G) to 7-segment display
4. Download and verify your design
   - Debug, re-synthesize, and re-download as needed
   - If Step 2 was carried out properly, this step may be unnecessary
5. Demonstrate your working circuit to the GTA

Questions and Report

1. Just by looking, would it have been easier to implement the circuit using POS equations for all outputs? What about just some outputs?
2. Based on your understanding of FPGA's, how would the SOP and a POS implementations of the above circuit differ when implemented on an FPGA?

Report Guidelines

1. Screenshot of your verified schematic
2. Screenshot of your ModelSim simulation results
3. All of your pre-lab work
4. Answers to questions