

Configuration of Virtex I and Spartan II

Internal Configuration Registers

Command Register (CMD) – used to execute configuration commands including:

- Reset CRC register (RCRC) used for error detection during download

- Change configuration clock (CCLK) frequency (SWITCH)

- Write configuration data (WCFG)

- Read configuration data (RCFG)

- Last frame write (LFRM)

- Begin start-up sequence (START)

- Asserts DONE signal, activates I/O buffers, de-asserts Global Set Reset (GSR) and Global Tri-State (GTS), and asserts Global Write Enable (GWE)

Frame Length Register (FLR) – used to specify frame size (number of bits that get loaded into the configuration memory frames). This allows all Virtex I and Spartan II devices to have identical configuration logic but means another instruction to be applied by users.

Configuration Option Register (COR) – used to specify user selected options including:

- Configuration rate (MHz)

- Start-up clock (CCLK, User clock, TCK from boundary scan interface)

- Number of clock cycles for various cycles (Done, GSR, GTS, GWE, and Lock for DLLs)

- Persist – whether configuration pins (like CCLK and Done) become user I/O after configuration (note that M0-2 and boundary scan interface pins are dedicated pins and cannot be changed)

- Security levels – to restrict access to configuration and readback operations:

 - None – no restrictions, i.e., we can always read the configuration memory

 - Level 1 – disables readback via boundary scan interface

 - Level 2 – disables readback from all possible ports (must active Program to override but this erases configuration memory)

- User ID – specifies the value of a 32-bit register accessible via the boundary scan USERCODE instruction

Control Register (CTL) – used to control internal functions including persist and security

Mask Register (MASK) – a safety mechanism that determines which bits in CTL can be modified after configuration

Frame Address Register (FAR) – used to specify the starting frame address for the next configuration data write cycle

Frame Data Register Input (FDRI) – writing to this register writes the contents of the configuration memory at the frame address specified by the FAR. After the write operation, the FDRI increments the FAR to next frame address (this allows continuous flow of configuration data during full configuration of the FPGA without the need to write the FAR between frames).

Frame Data Register Output (FDRO) – works like the FDRI but is used for outgoing frame data during readback of the configuration memory

CRC Register (CRC) – used to load the 16-bit CRC value embedded in the configuration bit-stream and compared to the internally generated CRC as the FPGA is configured to detect errors during download. The CRC characteristic polynomial for Virtex I and Spartan II is $P(x) = x^{16} + x^{15} + x^2 + 1$ and uses an internal feedback LFSR implementation.

Configuration Process Flow and File Format Example

Initialization	1 or more 32-bit dummy words	0xFFFFFFFF
Synchronization	1 fixed 32-bit word	0xAA995566
Command Register	1 fixed 32-bit word	0x30008001
Reset CRC	RCRC command	0x00000007
Frame Length Register	1 fixed 32-bit word	0x30016001
Set frame length	a 32-bit word specify frame size	0x000000--
Config Option Reg	1 fixed 32-bit word	0x30012001
Set options in COR (control parameters and CCLK frequency)		0x-----
Mask Register	1 fixed 32-bit word	0x3000C001
Write MASK	a 32-bit word for mask data	0x00000000
Frame Address Register	1 fixed 32-bit word	0x30002001
Set initial frame address	a 32-bit word for frame address	0x00000000
Command Register	1 fixed 32-bit word	0x30008001
Write config data	WCFG command	0x00000001
Frame Data Reg Input	1 fixed 32-bit word	0x30004000
Configuration Data	many 32-bits words	0x-----
.		
.		
.		
Command Register	1 fixed 32-bit word	0x30008001
Initiate Start-up Sequence	START command	0x00000005
Control Register	1 fixed 32-bit word	0x3000A001
Write Control Commands	a 32-bits word	0x00000000
CRC Register	1 fixed 32-bit word	0x30000001
Write CRC value	a 32-bits word from bit file	0x-----

Partial reconfiguration requires writes to the FAR with the starting frame address to be written with each write to the FAR followed by writes to FDRI for the number of consecutive frames to be written.

Configuration memory readback requires setting the FAR for the first address to be read, activating the RCFG command, and addressing the FDRO. Configuration memory data is then read during subsequent clock cycles.

When performing configuration memory readback for verification of a correct download to the FPGA, a mask file is required to indicate which configuration memory bits should be ignored as a result of the possibility of data changes in flip-flops and RAMs (both LUT-RAMs and block RAMs). This mask file can be optionally produced when generating the bit file to be downloaded.