Timing Issues

- Normally only steady-state behavior considered
- But transient behavior can also be important
  - Behavior may differ from steady state expectations
- Gates have finite delays
  - Unit gate delay (1 unit of delay per gate)
  - Propagation delay (gate delay $\propto$ gate size)
- Delays differ through various paths
  - Can lead to ‘glitches’ on combinational logic outputs
    - Called timing hazards (or just hazards, with timing implied)
      - Static-1 hazard: produces a glitch to logic 0
      - Static-0 hazard: produces a glitch to logic 1
Static Hazards

• **Definitions:**
  - Static-1 hazard caused by a pair of input values that:
    1. Differ by only one input variable (distance = 1),
    2. Both produce a logic 1 output, *and*
    3. Cause a momentary logic 0 (also called a 0 glitch) at the output during a transition from one input value to the other
  - Static-0 hazard caused by a pair of input values that:
    1. Differ by only one input variable (distance = 1),
    2. Both produce a logic 0 output, *and*
    3. Cause a momentary logic 1 (also called a 1 glitch) at the output during a transition from one input value to the other

• **Important properties:**
  - A properly designed 2-level AND-OR (SOP) circuit has no static-0 hazards, but may have static-1 hazards
  - A properly designed 2-level OR-AND (POS) circuit has no static-1 hazards, but may have static-0 hazards
Static-1 Hazard Example

**Multiplexer logic diagram**

- A
- S
- B
- Z
- \( AS' \)
- \( BS \)
- \( AB \)

\[ Z = AS' + BS \]

**Timing diagram**

- A
- B
- S
- S'
- \( AS' \)
- \( BS \)
- Z

\[ Z = AS' + BS + AB \]

**Note:** this group removes hazard

Hazard-free multiplexer output

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