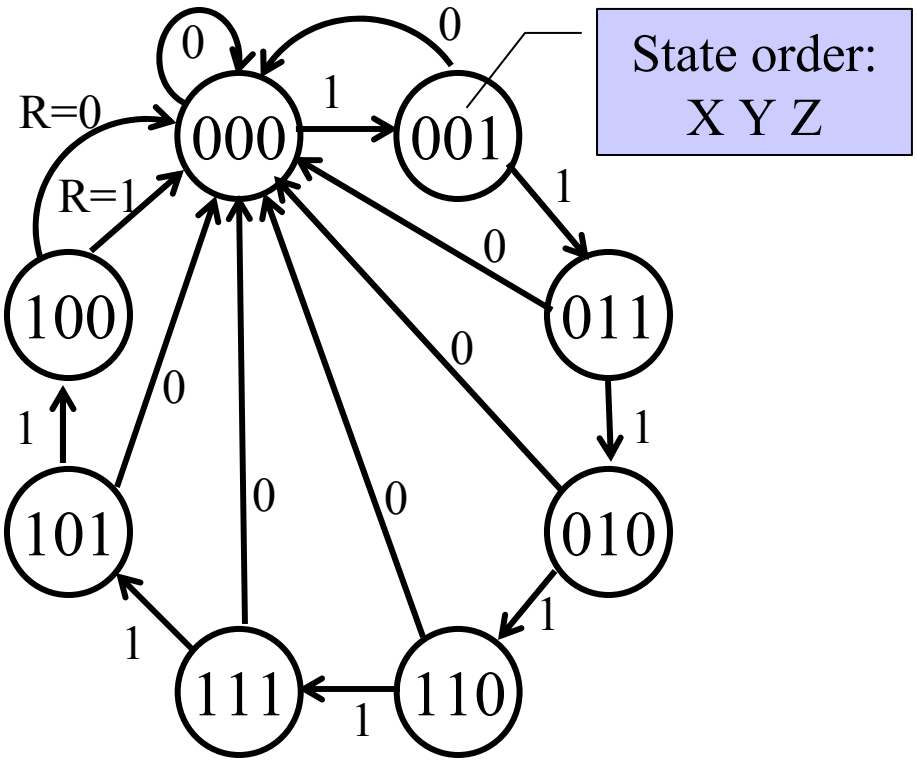
Basic Sequential Design Steps

- Derive circuit state diagram from design specs
- Create state table
- Choose flip-flops
- Create circuit excitation table
- Construct K-maps for:
  - flip-flop inputs
  - primary outputs
- Obtain minimized SOP equations
- Draw logic diagram
- Simulate to verify design & debug as needed
- Perform circuit analysis & logic optimization

Sequential Design Example

Design a 3-bit gray code counter with
active low synchronous reset (R)

State Diagram



Inputs R	Current state (X Y Z)	Next state (X Y Z)
0	XXX	000
1	000	001
1	001	011
1	010	110
1	011	010
1	100	000
1	101	100
1	110	111
1	111	101

State Table

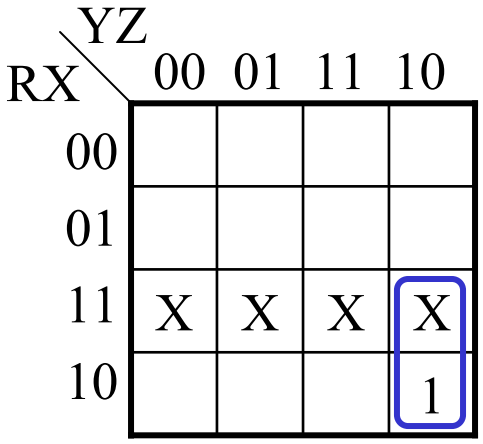
3-bit Gray Code Counter

- Choose flip-flops:
  - Let X be a JK
  - Let Y be a D
  - Let Z be a SR
- Create circuit excitation table

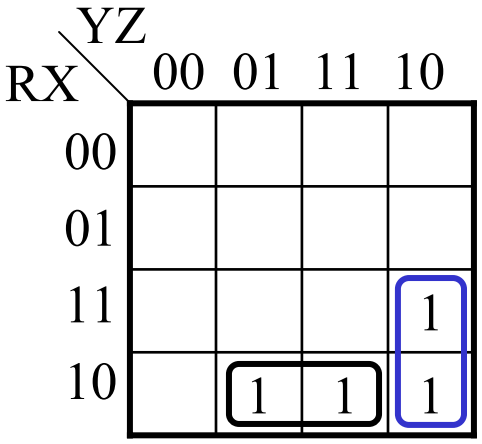
Inputs R	Current state (X Y Z)	Next state (X Y Z)	QX Jx Kx	QY Dy	QZ Sz Rz
0	X X X	0 0 0	0 1	0	0 1
1	0 0 0	0 0 1	0 X	0	1 0
1	0 0 1	0 1 1	0 X	1	X 0
1	0 1 0	1 1 0	1 X	1	0 X
1	0 1 1	0 1 0	0 X	1	0 1
1	1 0 0	0 0 0	X 1	0	0 X
1	1 0 1	1 0 0	X 0	0	0 1
1	1 1 0	1 1 1	X 0	1	1 0
1	1 1 1	1 0 1	X 0	0	X 0

3-bit Gray Code Counter (cont)

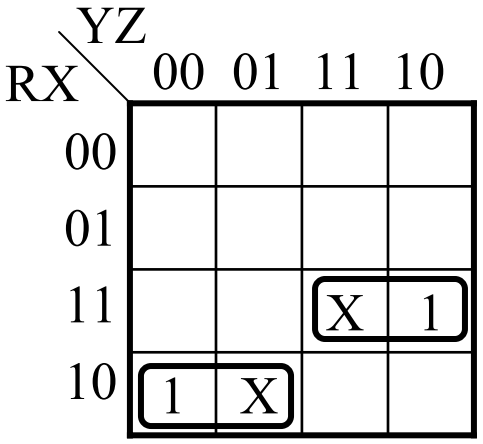
- Generate K-Maps & obtain minimized SOPs



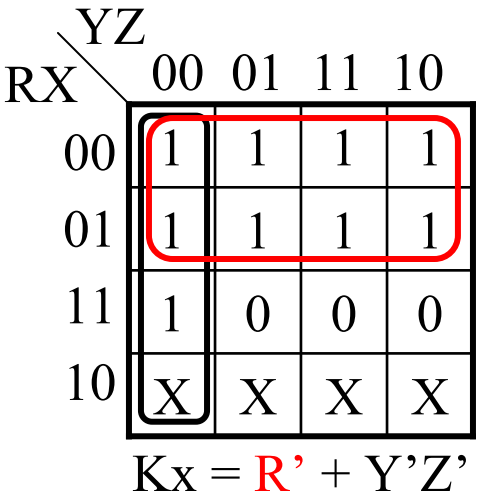
Jx = RYZ'



Dy = RYZ' + RX'Z



Sz = RXY + RX'Y'



Kx = R' + Y'Z'

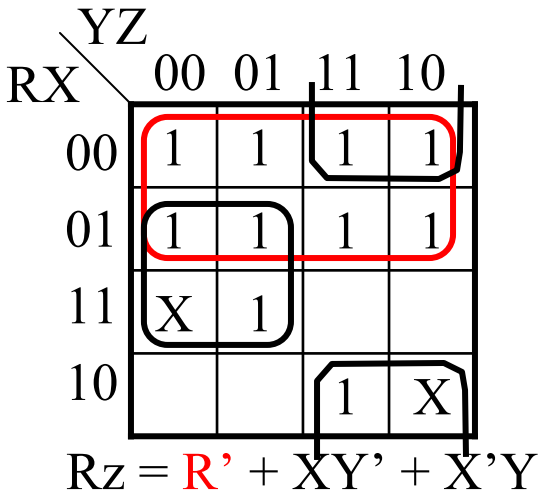
Further reductions:

Rz = R' + X⊕Y

Sz = R(X⊕Y)'

= (R' + X⊕Y)'

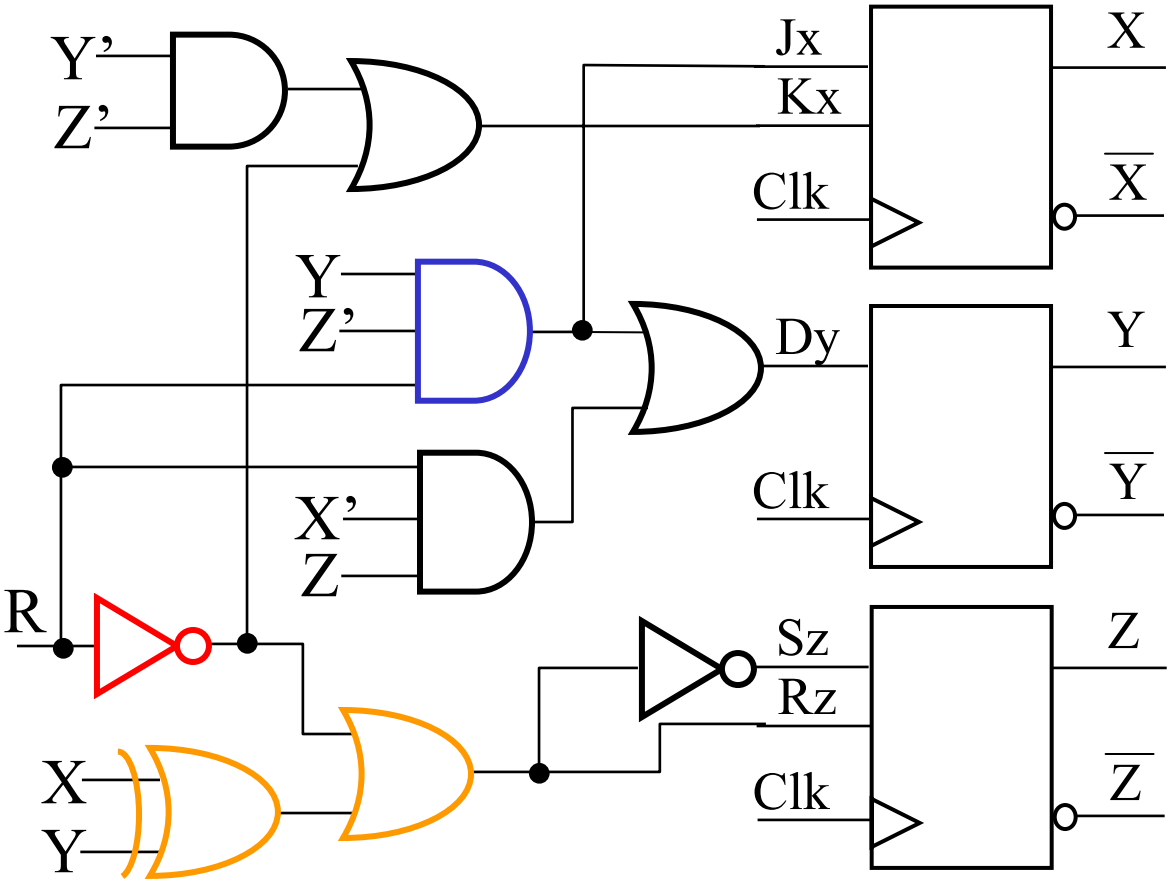
= Rz'



Rz = R' + XY' + X'Y

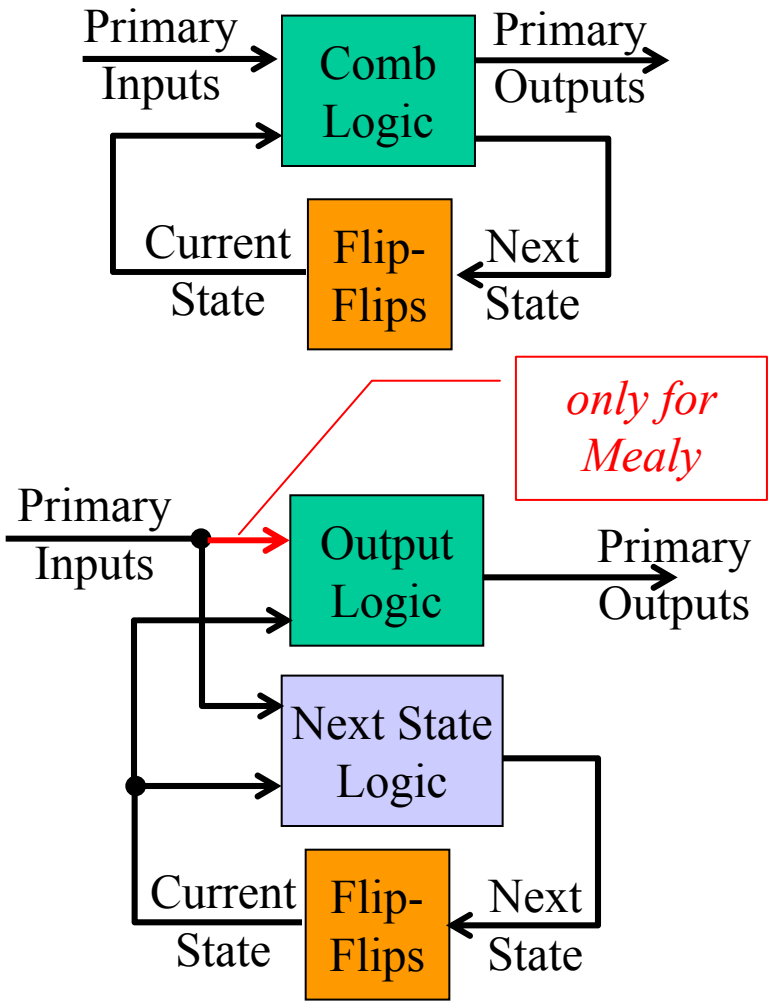
3-bit Gray Code Counter (cont)

- Logic diagram
- Next would come design verification via logic simulation
  - Debug as necessary to obtain working circuit
  - Update logic diagram, logic equations, etc. to reflect fixes



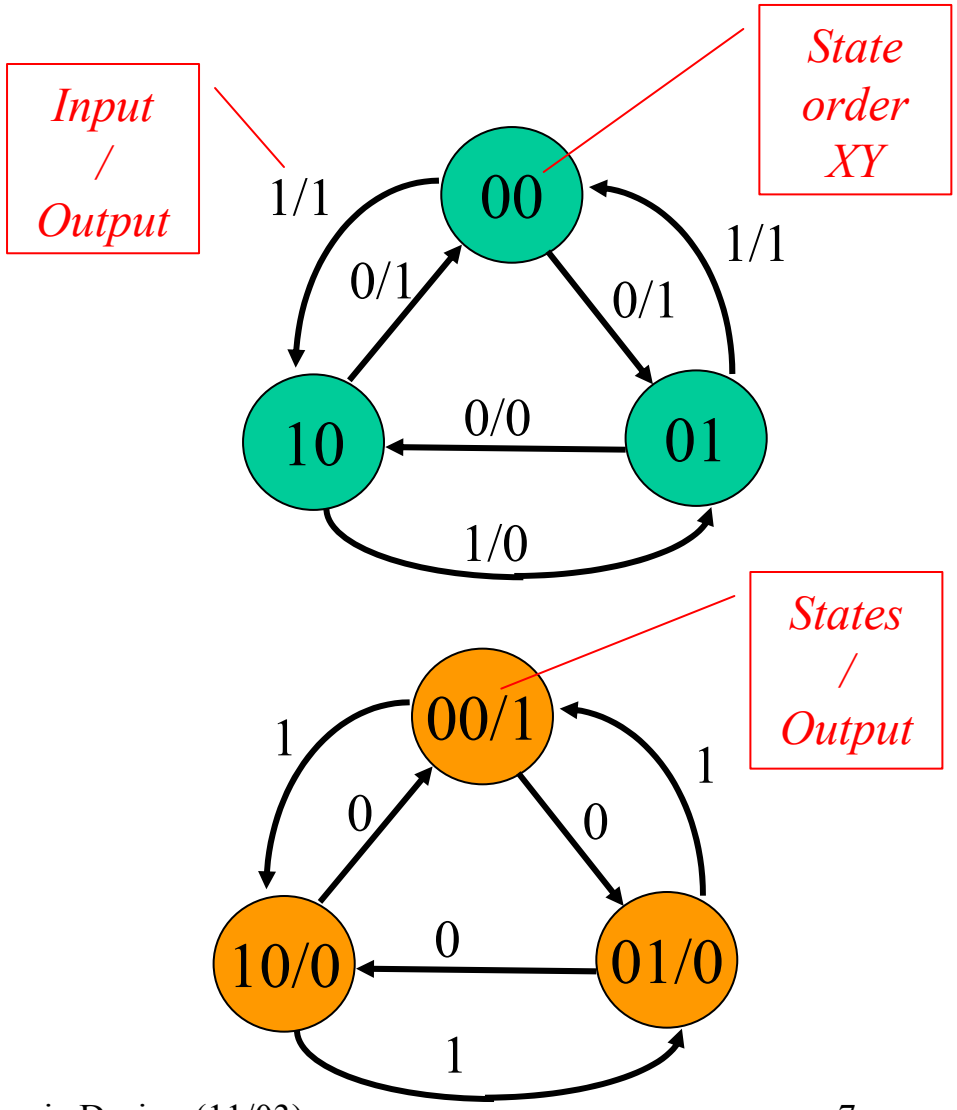
Sequential Logic Models

- Huffman model consists of two types:
  - ➢ Mealy model (aka Mealy machine)
    - Outputs are function inputs and current state
      - ✓ Outputs can change when inputs change or when current state changes
  - ➢ Moore model (aka Moore machine)
    - Outputs are function of current state only
      - ✓ Outputs can change only when current state changes

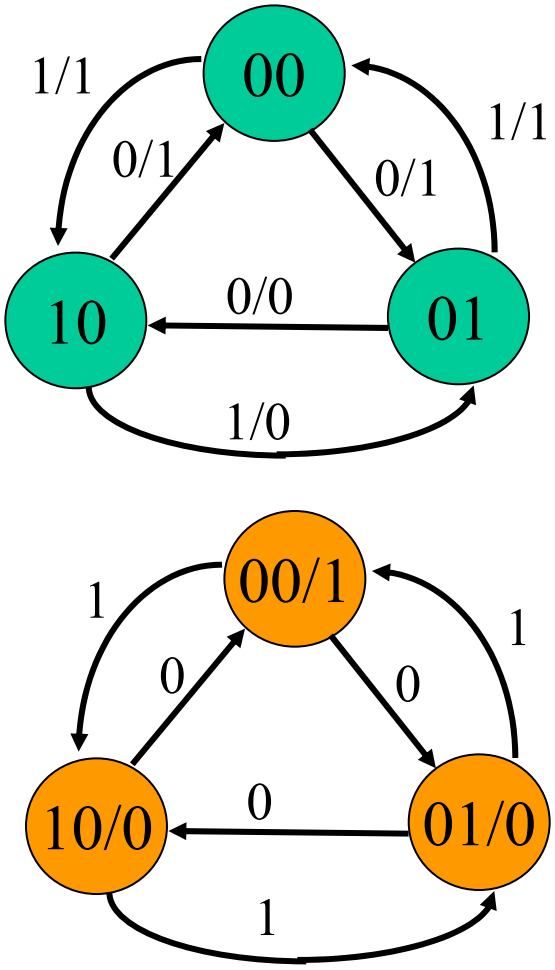


Mealy & Moore State Diagrams

- Mealy model
  - Outputs associated with state transition
  - Output values shown with inputs
- Moore model
  - Outputs associated with states only
  - Output values shown with states



Mealy & Moore State Tables



In	X	Y	X^+	Y^+	D_X	D_Y	O_{Mealy}	O_{Moore}
0	0	0	0	1	0	1	1	1
0	0	1	1	0	1	0	0	0
0	1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	1	1
1	0	1	0	0	0	0	1	0
1	1	0	0	1	0	1	0	0
0	1	1	X	X	X	X	X	X

Note: next state (next state logic) is same for both Mealy & Moore – only output is different

Mealy & Moore Design Examples

In \ XY	00	01	11	10
0	0	1	X	0
1	1	0	X	0

$D_X = In'Y + InX'Y'$

In \ XY	00	01	11	10
0	1	0	X	1
1	1	1	X	0

$O_{Mealy} = In'Y' + InX'$

In \ XY	00	01	11	10
0	1	0	X	0
1	0	0	X	1

$D_Y = InX + In'X'Y'$

In \ XY	00	01	11	10
0	1	0	X	0
1	1	0	X	0

$O_{Moore} = X'Y'$

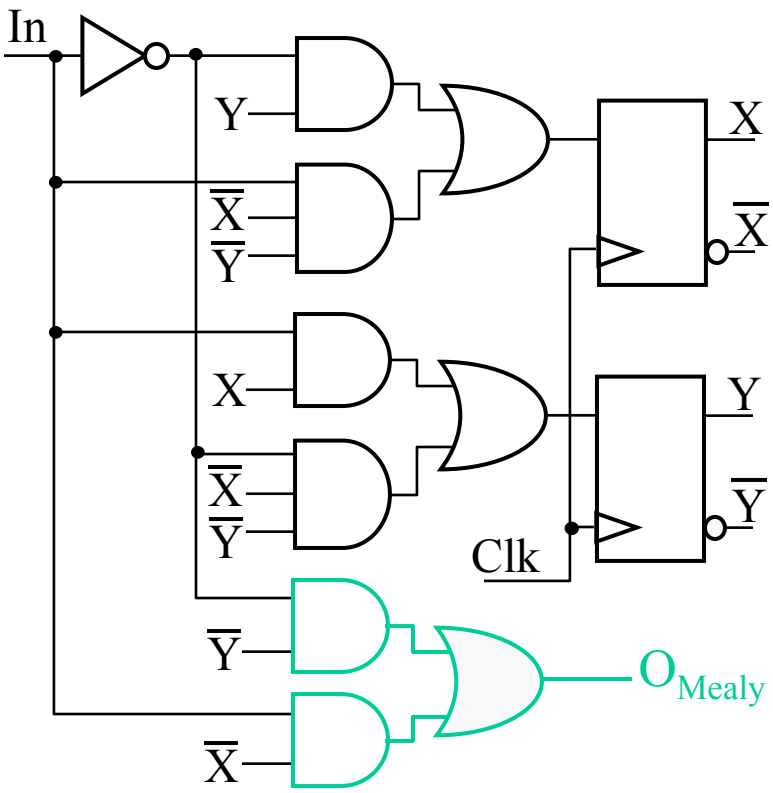
Mealy & Moore Design Examples

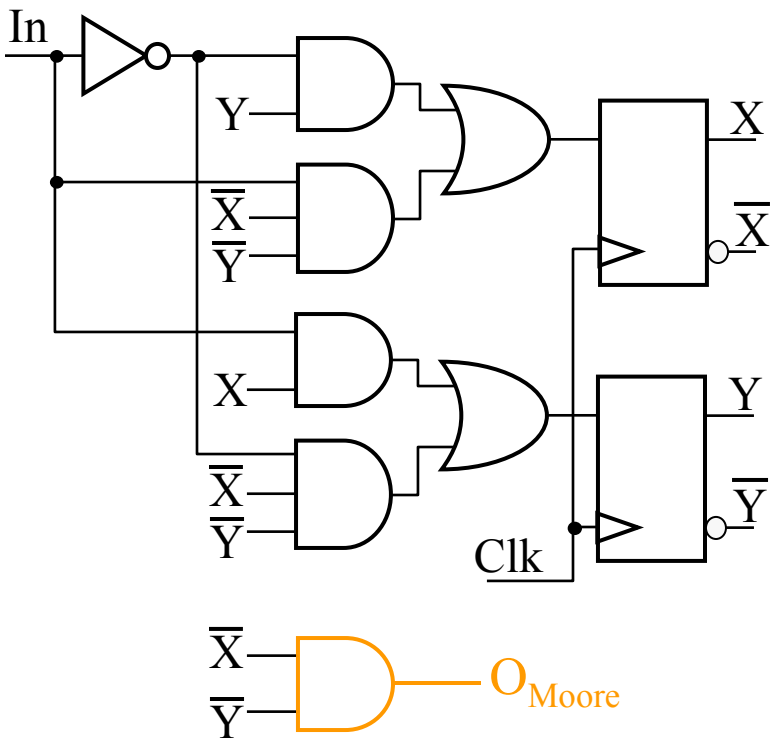
$O_{Mealy} = In'Y' + InX'$

$D_X = In'Y + InX'Y'$

$D_Y = InX + In'X'Y'$

$O_{Moore} = X'Y'$





Note: O_{Mealy} ***is*** a function of In but O_{Moore} ***is not*** a function of In