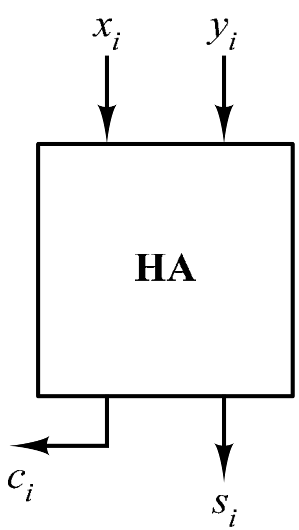
Half Adders

no carry-in

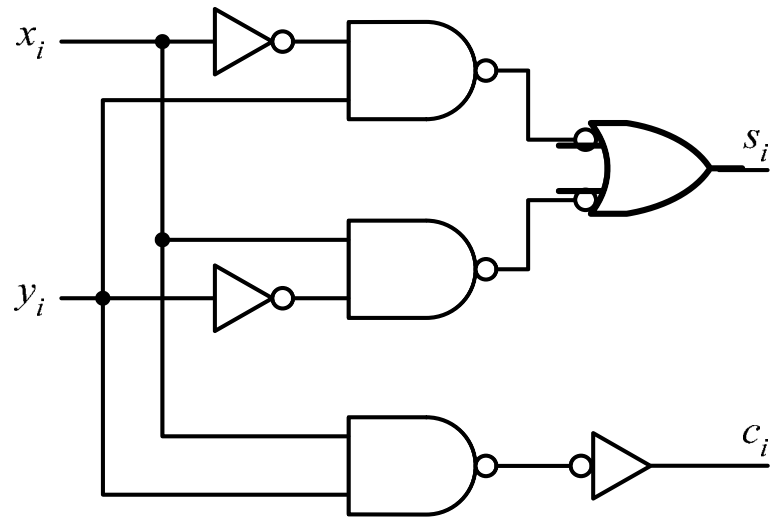
$$HA \begin{cases} s_i = x_i \oplus y_i \\ c_i = x_i \bullet y_i \end{cases}$$



(a)

x_i	y_i	c_i	s_i
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(b)

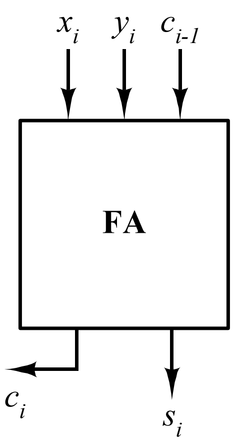


(c) NAND gate HA

Full Adders

with carry-in

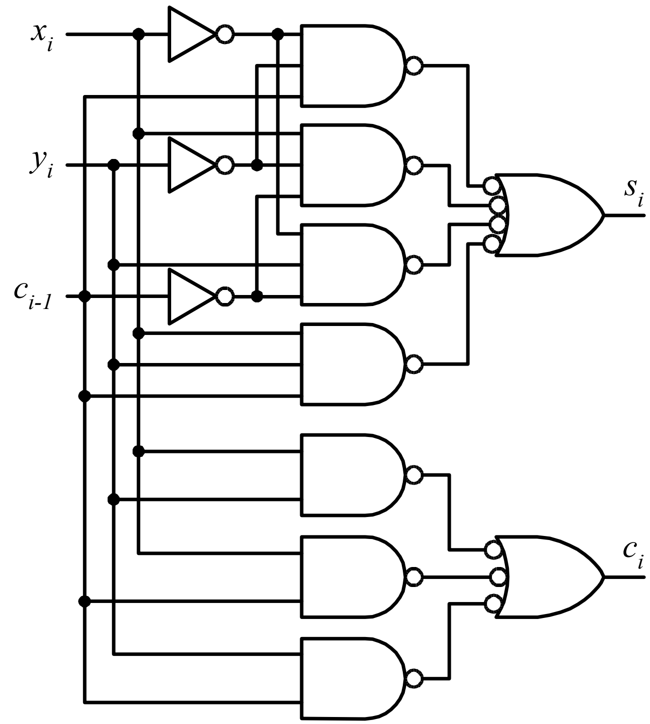
$$FA \begin{cases} s_i = x_i \oplus y_i \oplus c_{i-1} \\ c_i = x_i \bullet y_i + x_i \bullet c_{i-1} + y_i \bullet c_{i-1} \end{cases}$$



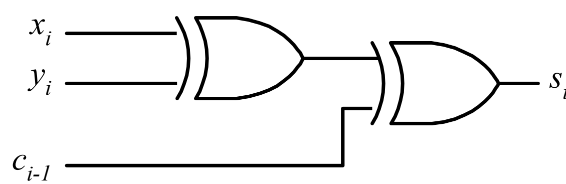
(d)

x_i	y_i	c_{i-1}	c_i	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(e)



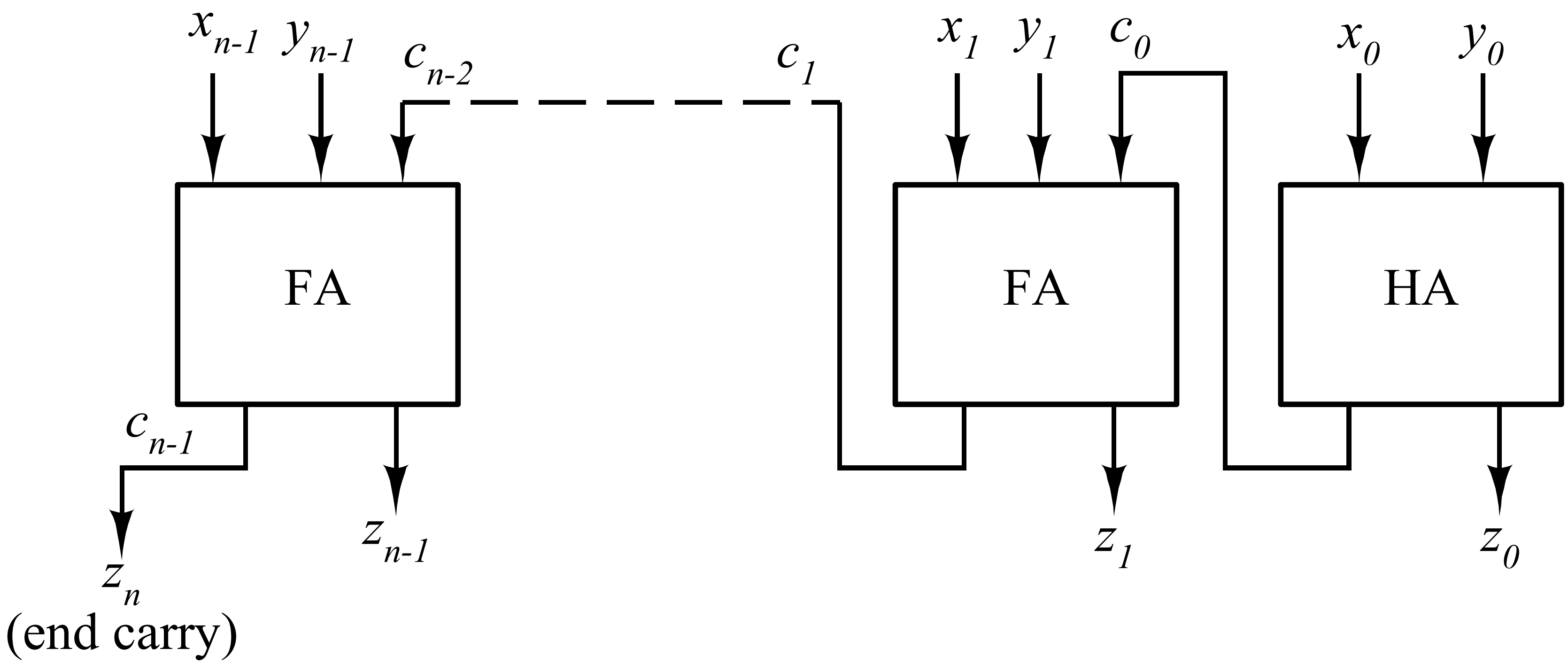
(f)



(g)

Ripple Carry Adder

slow, less hard ware



Delay in Ripple-Carry Adder

Let t_{gate} = propogation delay through a logic gate, assuming the same delay for inverters (normally inverter has less delay).

Half adder propagation delays

$t_{add} = 3\ t_{gate}$
$t_{carry} = 1\ t_{gate}$

$$HA \begin{cases} s_i = x_i \oplus y_i \\ c_i = x_i \bullet y_i \end{cases}$$

Full adder propagation delays

$t_{add} = 3\ t_{gate}$
$t_{carry} = 2\ t_{gate}$

$$FA \begin{cases} s_i = x_i \oplus y_i \oplus c_{i-1} \\ c_i = x_i \bullet y_i + x_i \bullet c_{i-1} + y_i \bullet c_{i-1} \end{cases}$$

Ripple-Carry Adder (*n*-bits)

$t_{add} = [1+(n - 2)2]\ t_{gate} + 3\ t_{gate}$
$= 2n *\ t_{gate}$

Fully Parallel Three-Bit Adder

Use minimal level of logic to achieve fast speed

$$c_0 = x_0 y_0 \qquad (4.30)$$

$$s_0 = x_0 \oplus y_0$$

$$c_1 = x_1 y_1 c_0' + x_1 y_1 c_0 + x_1 y_1' c_0 + x_1' y_1 c_0$$

$$= x_1 y_1 + (x_1 \oplus y_1) c_0$$

$$= x_1 y_1 + (x_1 \oplus y_1)(x_0 y_0) \qquad (4.31)$$

$$s_1 = x_1 \oplus y_1 \oplus c_0$$

$$= x_1 \oplus y_1 \oplus x_0 y_0$$

$$c_2 = x_2 y_2 + (x_2 \oplus y_2) c_1$$

$$= x_2 y_2 + (x_2 \oplus y_2)[x_1 y_1 + (x_1 \oplus y_1)(x_0 y_0)] \qquad (4.32)$$

$$s_2 = x_2 \oplus y_2 \oplus c_1$$

$$= x_2 \oplus y_2 \oplus [x_1 y_1 + (x_1 \oplus y_1)(x_0 y_0)]$$

Delay for a Fully Parallel Adder

Assuming a three-level realization:

$$t_{add} = 3\, t_{gate}$$

However, the fan in requirements become impractical as *n* increases.

Gate count large, cost high.

Carry Look-Ahead Adders -- Basic Idea

Recall that

$$c_i = x_i y_i + x_i c_{i-1} + y_i c_{i-1} = x_i y_i + (x_i + y_i) c_{i-1}$$

$$= x_i y_i + x_i y_i c_{i-1} + x_i y_i' c_{i-1} + x_i y_i c_{i-1} + x_i' y_i c_{i-1}$$

$$= x_i y_i + x_i y_i' c_{i-1} + x_i' y_i c_{i-1}$$

$$= x_i y_i + (x_i y_i' + x_i' y_i) c_{i-1}$$

$$= x_i y_i + (x_i \oplus y_i) c_{i-1}$$

Let

$g_i = x_i y_i$ **[carry generate]**

$p_i = x_i \oplus y_i$ **[carry propagate]**

Then

$$c_i = g_i + p_i c_{i-1}$$

$$s_i = p_i \oplus c_{i-1}$$

3 Bit Carry Look-Ahead Adders

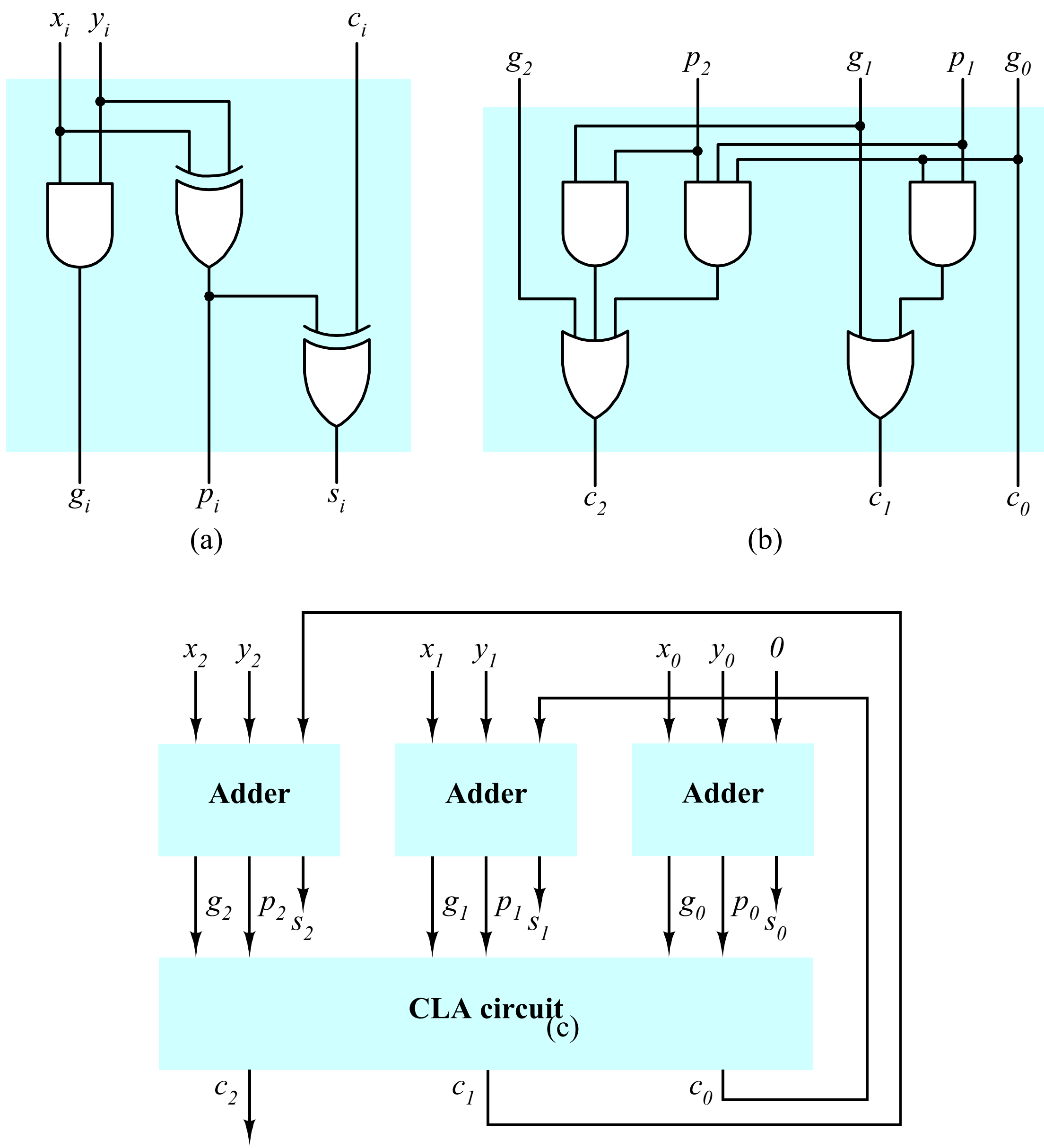
First Level Abstraction

$$c_0 = g_0 \qquad (4.35)$$
$$s_0 = p_0$$

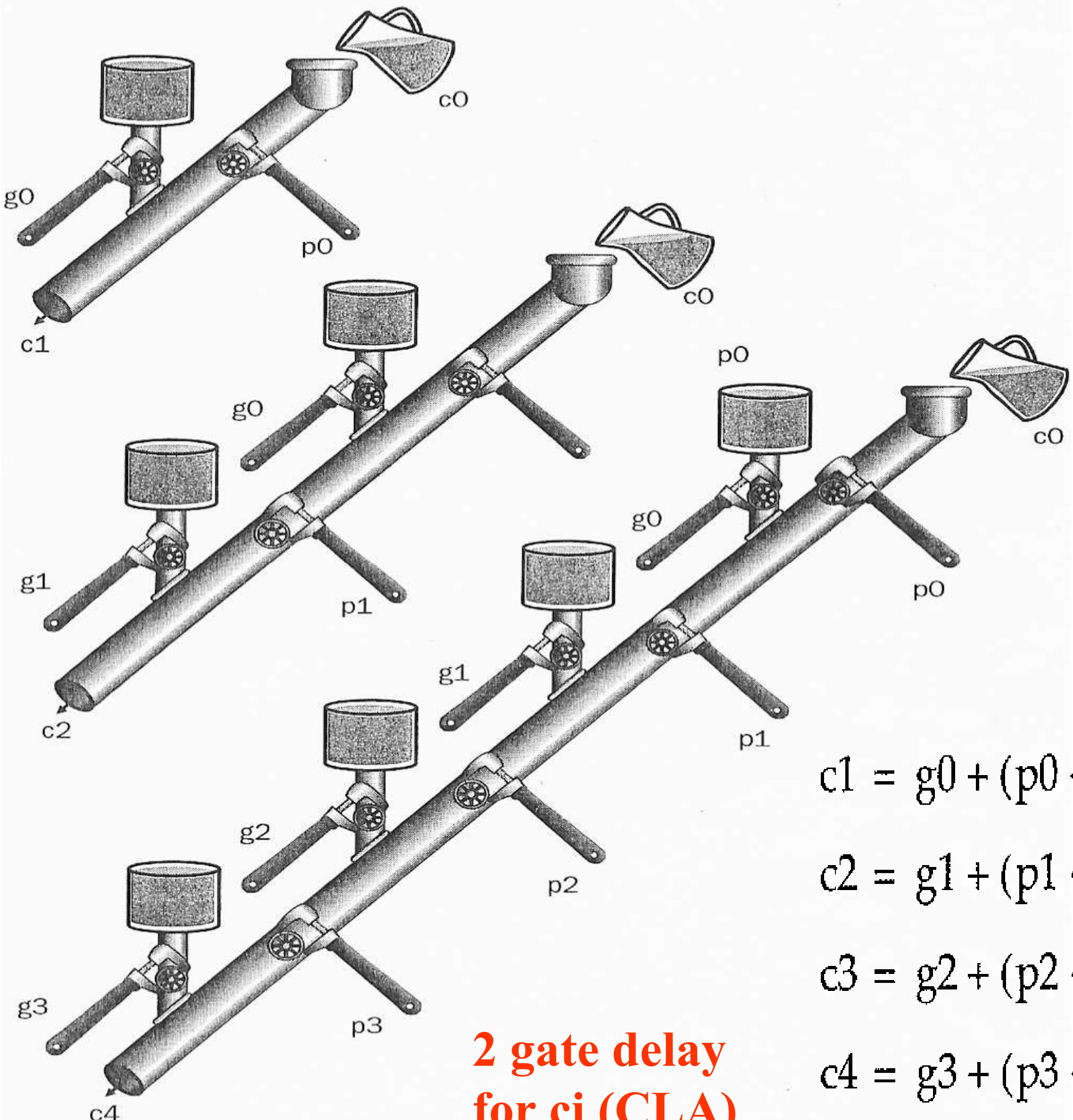
$$c_1 = g_1 + p_1 c_0$$
$$= g_1 + p_1 g_0 \qquad (4.36)$$
$$s_1 = p_1 \oplus c_0$$

$$c_2 = g_2 + p_2 c_1$$
$$= g_2 + p_2(g_1 + p_1 g_0)$$
$$= g_2 + p_2 g_1 + p_2 p_1 g_0 \qquad (4.37)$$
$$s_2 = p_2 \oplus c_1$$

First Level 3 Bit Carry Look-Ahead Adder



4 Bit Carry Look-Ahead Adders



First Level Abstraction

$$g_i = x_i y_i$$
$$p_i = x_i \oplus y_i$$

1 gate delay for pi & gi

2 gate delay for ci (CLA)

$$c1 = g0 + (p0 \cdot c0)$$

$$c2 = g1 + (p1 \cdot g0) + (p1 \cdot p0 \cdot c0)$$

$$c3 = g2 + (p2 \cdot g1) + (p2 \cdot p1 \cdot g0) + (p2 \cdot p1 \cdot p0 \cdot c0)$$

$$c4 = g3 + (p3 \cdot g2) + (p3 \cdot p2 \cdot g1) + (p3 \cdot p2 \cdot p1 \cdot g0) + (p3 \cdot p2 \cdot p1 \cdot p0 \cdot c0)$$

Delay for First Level Carry Look-Ahead Adder

Adder modules (assuming XOR=2 gate delay, inverter has no delay)

$t_g = t_{gate}$, $t_p = t_s = 2t_{gate}$ $gi = x_i y_i$, $pi = x_i \oplus y_i$ $s_i = p_i \oplus c_{i-1}$

CLA module

$$c1 = g0 + (p0 \cdot c0)$$
$$c2 = g1 + (p1 \cdot g0) + (p1 \cdot p0 \cdot c0)$$
$$c3 = g2 + (p2 \cdot g1) + (p2 \cdot p1 \cdot g0) + (p2 \cdot p1 \cdot p0 \cdot c0)$$
$$c4 = g3 + (p3 \cdot g2) + (p3 \cdot p2 \cdot g1) + (p3 \cdot p2 \cdot p1 \cdot g0) + (p3 \cdot p2 \cdot p1 \cdot p0 \cdot c0)$$

$t_c = 2\ t_{gate}$

Overall

$$t_{add} = 2t_{gate}\ (\text{p \& g}) + 2\ t_{gate}\ (\text{CLA}) + 2t_{gate}\ (\text{Sum}) = 6\ t_{gate}$$

$C_{HA} + C_{FA}$ $+\ SUM_{lastbit}$

Ripple Adder Delay = [1 + (n - 2)2] t_{gate} + $2t_{gate}$ = (2n-1)* t_{gate}

$$HA \begin{cases} s_i = x_i \oplus y_i \\ c_i = x_i \bullet y_i \end{cases} \qquad FA \begin{cases} s_i = x_i \oplus y_i \oplus c_{i-1} \\ c_i = x_i \bullet y_i + x_i \bullet c_{i-1} + y_i \bullet c_{i-1} \end{cases}$$

Full Parallel Adder Delay = $3t_{gate}$, assuming 3-level with infinite fan-in.

Delay for First Level Carry Look-Ahead Adder

Adder modules (assuming XOR=1 gate delay, inverter has no delay)

$$t_g = t_p = t_s = t_{gate} \qquad gi = x_i y_i,\ pi = x_i \oplus y_i \qquad s_i = p_i \oplus c_{i-1}$$

CLA module

$$\begin{aligned} c1 &= g0 + (p0 \cdot c0) \\ c2 &= g1 + (p1 \cdot g0) + (p1 \cdot p0 \cdot c0) \\ c3 &= g2 + (p2 \cdot g1) + (p2 \cdot p1 \cdot g0) + (p2 \cdot p1 \cdot p0 \cdot c0) \\ c4 &= g3 + (p3 \cdot g2) + (p3 \cdot p2 \cdot g1) + (p3 \cdot p2 \cdot p1 \cdot g0) \\ &\quad + (p3 \cdot p2 \cdot p1 \cdot p0 \cdot c0) \end{aligned}$$

$$t_c = 2\ t_{gate}$$

Overall

$$t_{add} = t_{gate}\ (\text{p \& g}) + 2\ t_{gate}\ (\text{CLA}) + t_{gate}\ (\text{Sum}) = 4\ t_{gate}$$

$$C_{HA} + C_{FA} \qquad + \ SUM_{lastbit}$$

Ripple Adder Delay =[1+(n - 2)2] t_{gate}+ t_{gate}

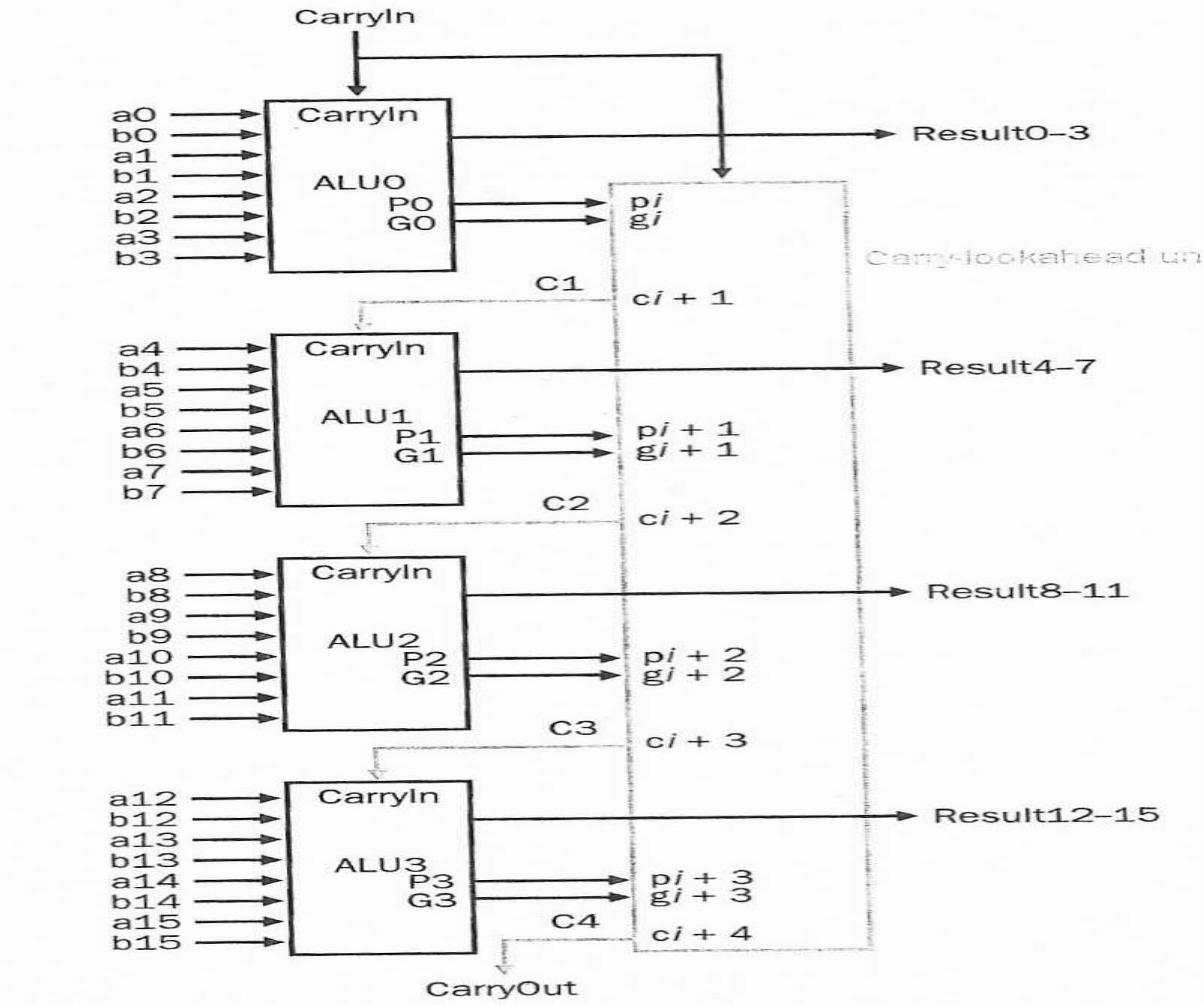
= 2(n-1)* t_{gate}

$$HA \begin{cases} s_i = x_i \oplus y_i \\ c_i = x_i \bullet y_i \end{cases}$$

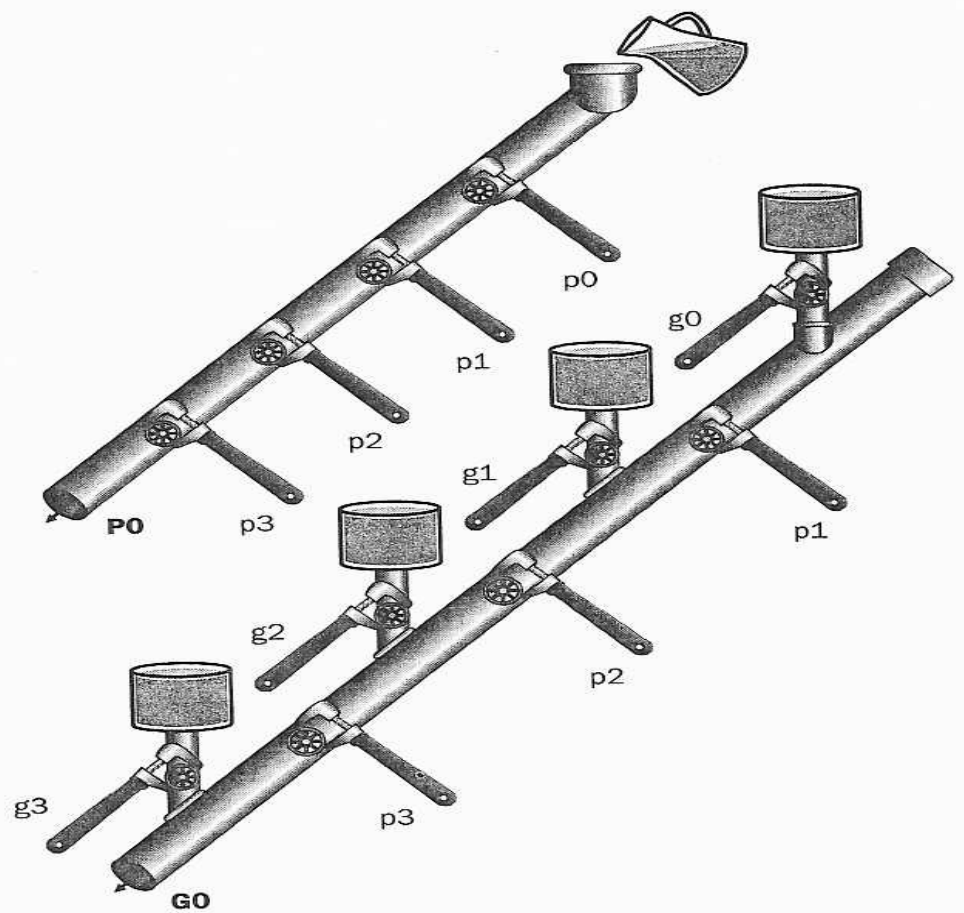
$$FA \begin{cases} s_i = x_i \oplus y_i \oplus c_{i-1} \\ c_i = x_i \bullet y_i + x_i \bullet c_{i-1} + y_i \bullet c_{i-1} \end{cases}$$

16 Bit Carry Look-Ahead Adders

Second Level Abstraction



16 Bit Carry Look-Ahead Adders



Second Level Abstraction

$$P0 = p3 \cdot p2 \cdot p1 \cdot p0$$

$$P1 = p7 \cdot p6 \cdot p5 \cdot p4$$

$$P2 = p11 \cdot p10 \cdot p9 \cdot p8$$

$$P3 = p15 \cdot p14 \cdot p13 \cdot p12$$

1 gate delay for Pi

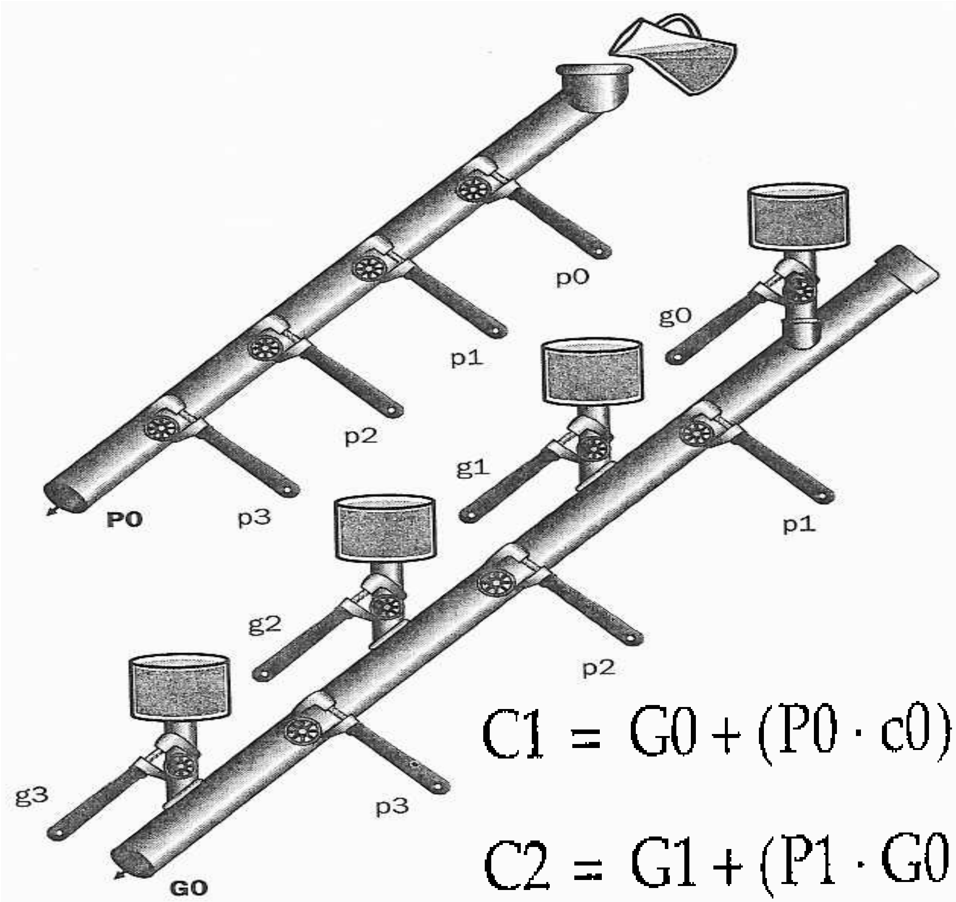
$$G0 = g3 + (p3 \cdot g2) + (p3 \cdot p2 \cdot g1) + (p3 \cdot p2 \cdot p1 \cdot g0)$$

$$G1 = g7 + (p7 \cdot g6) + (p7 \cdot p6 \cdot g5) + (p7 \cdot p6 \cdot p5 \cdot g4)$$

$$G2 = g11 + (p11 \cdot g10) + (p11 \cdot p10 \cdot g9) + (p11 \cdot p10 \cdot p9 \cdot g8)$$

$$G3 = g15 + (p15 \cdot g14) + (p15 \cdot p14 \cdot g13) + (p15 \cdot p14 \cdot p13 \cdot g12)$$

2 gate delay for Gi



16 Bit Carry Look-Ahead Adders

Second Level Abstraction

Delay for 2 level CLA=
1 gate delay for pi & gi +
2 gate delay for Pi & Gi +
2 gate delay for Ci +
2 gate delay for ci in last unit +
1 gate delay for sum

$$C1 = G0 + (P0 \cdot c0)$$

$$C2 = G1 + (P1 \cdot G0) + (P1 \cdot P0 \cdot c0)$$

$$C3 = G2 + (P2 \cdot G1) + (P2 \cdot P1 \cdot G0) + (P2 \cdot P1 \cdot P0 \cdot c0)$$

2 gate delay for Ci

$$C4 = G3 + (P3 \cdot G2) + (P3 \cdot P2 \cdot G1) + (P3 \cdot P2 \cdot P1 \cdot G0) + (P3 \cdot P2 \cdot P1 \cdot P0 \cdot c0)$$

Delay for Second Level Carry Look-Ahead Adder

Adder modules (assuming XOR=2 gate delay, inverter has no delay)

$t_g = t_{gate}, \; t_p = t_s = 2t_{gate}$ $\quad gi = x_i y_i, \; pi = x_i \oplus y_i \quad s_i = p_i \oplus c_{i-1}$

1st level CLA module: $t_{c1} = 2\, t_{gate}$

$$c1 = g0 + (p0 \cdot c0)$$
$$c2 = g1 + (p1 \cdot g0) + (p1 \cdot p0 \cdot c0)$$
$$c3 = g2 + (p2 \cdot g1) + (p2 \cdot p1 \cdot g0) + (p2 \cdot p1 \cdot p0 \cdot c0)$$
$$c4 = g3 + (p3 \cdot g2) + (p3 \cdot p2 \cdot g1) + (p3 \cdot p2 \cdot p1 \cdot g0) + (p3 \cdot p2 \cdot p1 \cdot p0 \cdot c0)$$

$$P0 = p3 \cdot p2 \cdot p1 \cdot p0$$
$$P1 = p7 \cdot p6 \cdot p5 \cdot p4$$
$$P2 = p11 \cdot p10 \cdot p9 \cdot p8$$
$$P3 = p15 \cdot p14 \cdot p13 \cdot p12$$

$$G0 = g3 + (p3 \cdot g2) + (p3 \cdot p2 \cdot g1) + (p3 \cdot p2 \cdot p1 \cdot g0)$$
$$G1 = g7 + (p7 \cdot g6) + (p7 \cdot p6 \cdot g5) + (p7 \cdot p6 \cdot p5 \cdot g4)$$
$$G2 = g11 + (p11 \cdot g10) + (p11 \cdot p10 \cdot g9) + (p11 \cdot p10 \cdot p9 \cdot g8)$$
$$G3 = g15 + (p15 \cdot g14) + (p15 \cdot p14 \cdot g13) + (p15 \cdot p14 \cdot p13 \cdot g12)$$

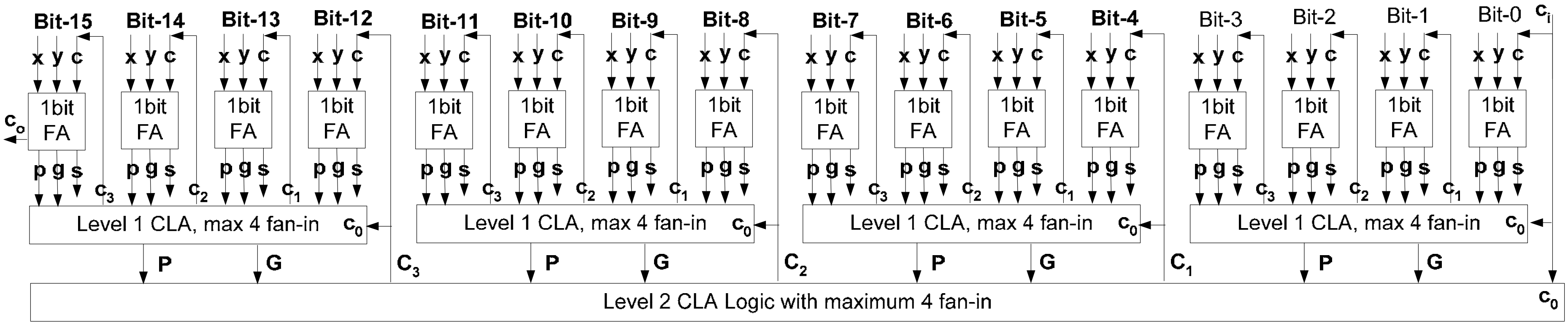
$$C1 = G0 + (P0 \cdot c0)$$
$$C2 = G1 + (P1 \cdot G0) + (P1 \cdot P0 \cdot c0)$$
$$C3 = G2 + (P2 \cdot G1) + (P2 \cdot P1 \cdot G0) + (P2 \cdot P1 \cdot P0 \cdot c0)$$
$$C4 = G3 + (P3 \cdot G2) + (P3 \cdot P2 \cdot G1) + (P3 \cdot P2 \cdot P1 \cdot G0) + (P3 \cdot P2 \cdot P1 \cdot P0 \cdot c0)$$

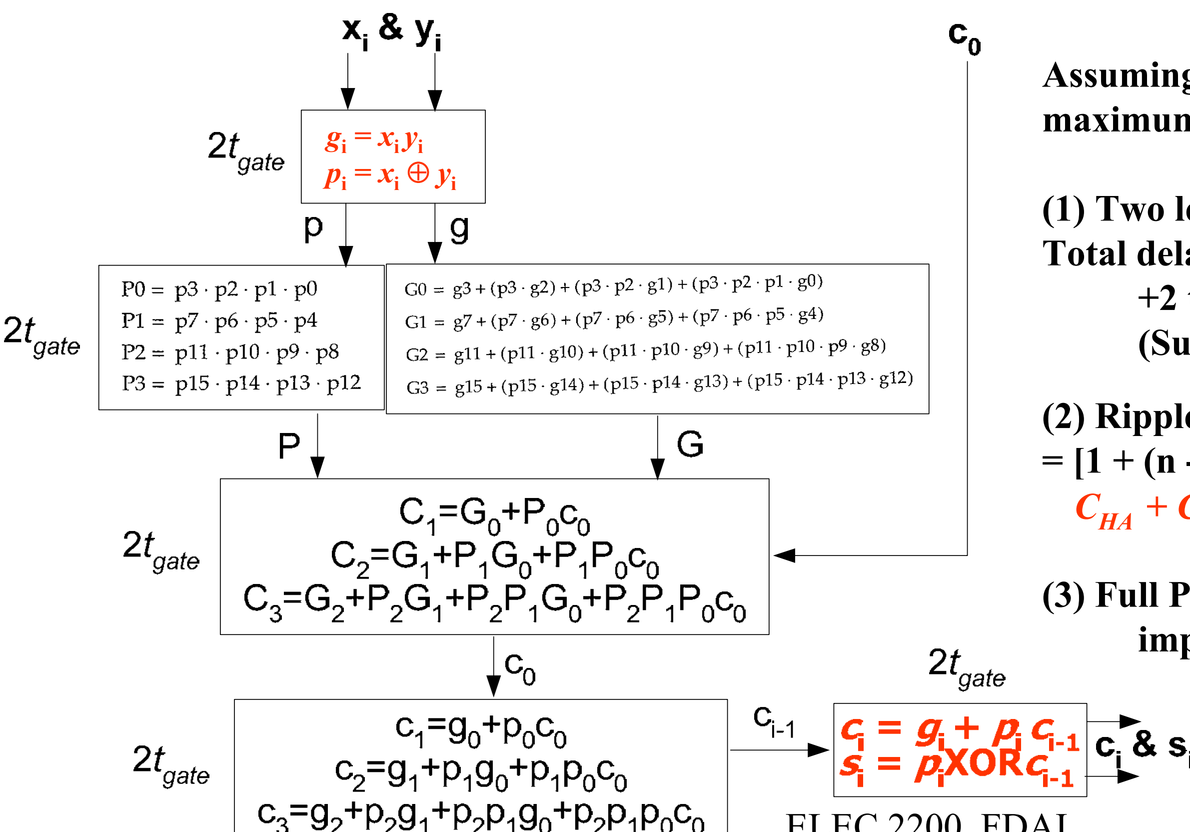
2nd level P, G module: $t_{P.G} = 2\, t_{gate}$

2nd level CLA module: $t_{c2} = 2\, t_{gate}$

Overall: $t_{add} = 2t_{gate}$ **(p & g) +** $2t_{gate}$ **(P & G) +** $2\, t_{gate}$ **(2nd CLA) +** $2\, t_{gate}$ **(1st CLA) +** $2t_{gate}$ **(Sum of MSB) =** $10\, t_{gate}$

A 16 Bit Adder with 2-level CLA Logic, max 4 fan-in, and 10 gate delay





Assuming XOR=2 gate delay, and maximum fan-in = 4 inputs.

(1) Two level CLA with 4 modules in one group.
Total delay: $t_{add} = 2t_{gate}$ **(p & g) +** $2t_{gate}$ **(P & G) +2** t_{gate} **(2**nd **CLA) +** $2t_{gate}$ **(1**st **CLA) +** $2t_{gate}$ **(Sum of MSB) = 10** t_{gate}

(2) Ripple Adder Delay:
$= [1 + (n - 2)2]\ t_{gate} + 2\ t_{gate} = (2n-1)^*\ t_{gate} = 31t_{gate}$
$C_{HA} + C_{FA}$ $+ SUM_{lastbit}$

(3) Full Parallel Adder Delay: cannot be implemented with 4-inputs.