

# On System-Level Use of BIST for Programmable Input/Output Buffers in FPGAs

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## Field Programmable Gate Arrays (FPGAs)

- Two dimensional array of complex configurable logic and routing resources
- Over 1 billion transistors in the largest FPGAs
- In-system reconfiguration to perform any digital function
- Excellent for digital baseband circuitry in RF applications and for software defined radios
- Reconfiguration offers inherent fault tolerant opportunities
- Size, programmability, and complexity pose serious testing problems

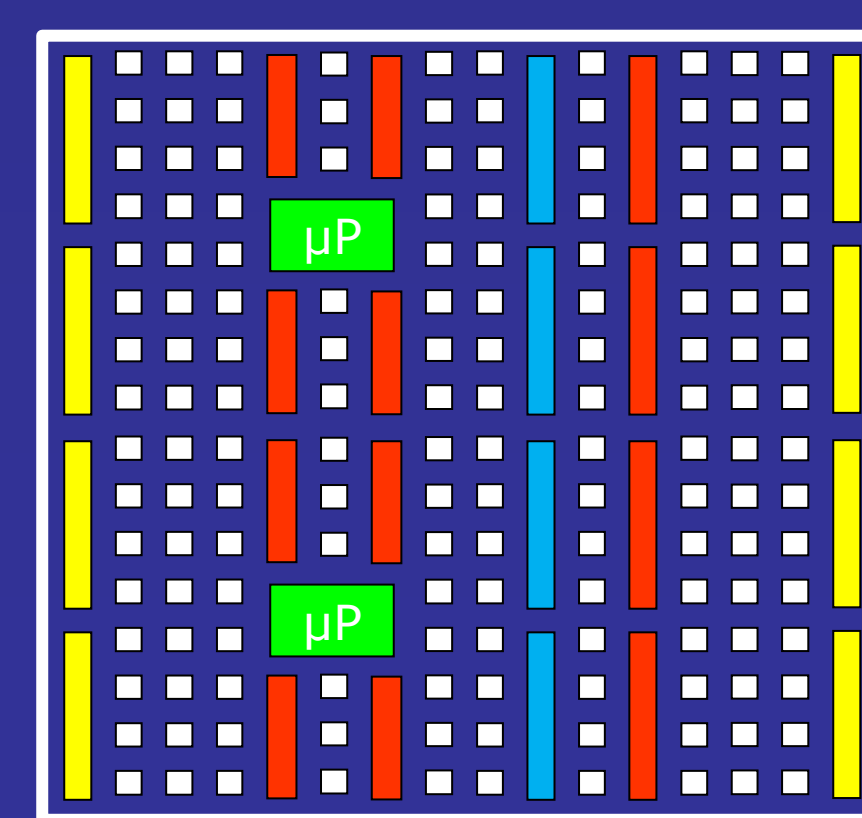
### FPGA Components

- Configurable logic blocks (CLB)
  - Up to 51,840 CLBs with 4 flip-flops and 4 6-input look-up tables
- Digital signal processors (DSP)
  - Up to 640 48-bit DSPs with 25x18-bit multiplier and 48-bit accumulator
- Random access memory (RAM)
  - Up to 648 18Kbit dual-port RAMs can operate as RAM or FIFO with error detection and correction
- Microprocessor cores ( $\mu$ P)
  - Up to 2 PowerPCs
  - FPGAs support synthesis of many soft core processors
- Up to 1200 Inputs/Outputs (I/O)
  - Support SDR and DDR
  - Serialization/Deserialization

## Built-In Self-Test (BIST)

- Design circuit to test itself to improve test/diagnosis and reduce test time/cost
- Requires test pattern generators (TPGs) and output response analyzers (ORAs)
- For FPGAs, reprogram device to test itself with no area overhead or performance penalty
- Program logic resources as TPGs and ORAs along with resources under test in the FPGA
- Multiple TPGs supply patterns to identically configured resources under test
- Comparison-based ORAs monitor responses and latch mismatches due to faults
- Result of test determined by configuration memory read back or overall single-bit pass/fail

Feature	AT94K	Virtex-4	Virtex-5
Multiplexers	4	32	32
Flip-flops/latches	2	10	10
Output drive levels	3	7	7
I/O standards	3	64	75
BIST Configurations	25	76	77



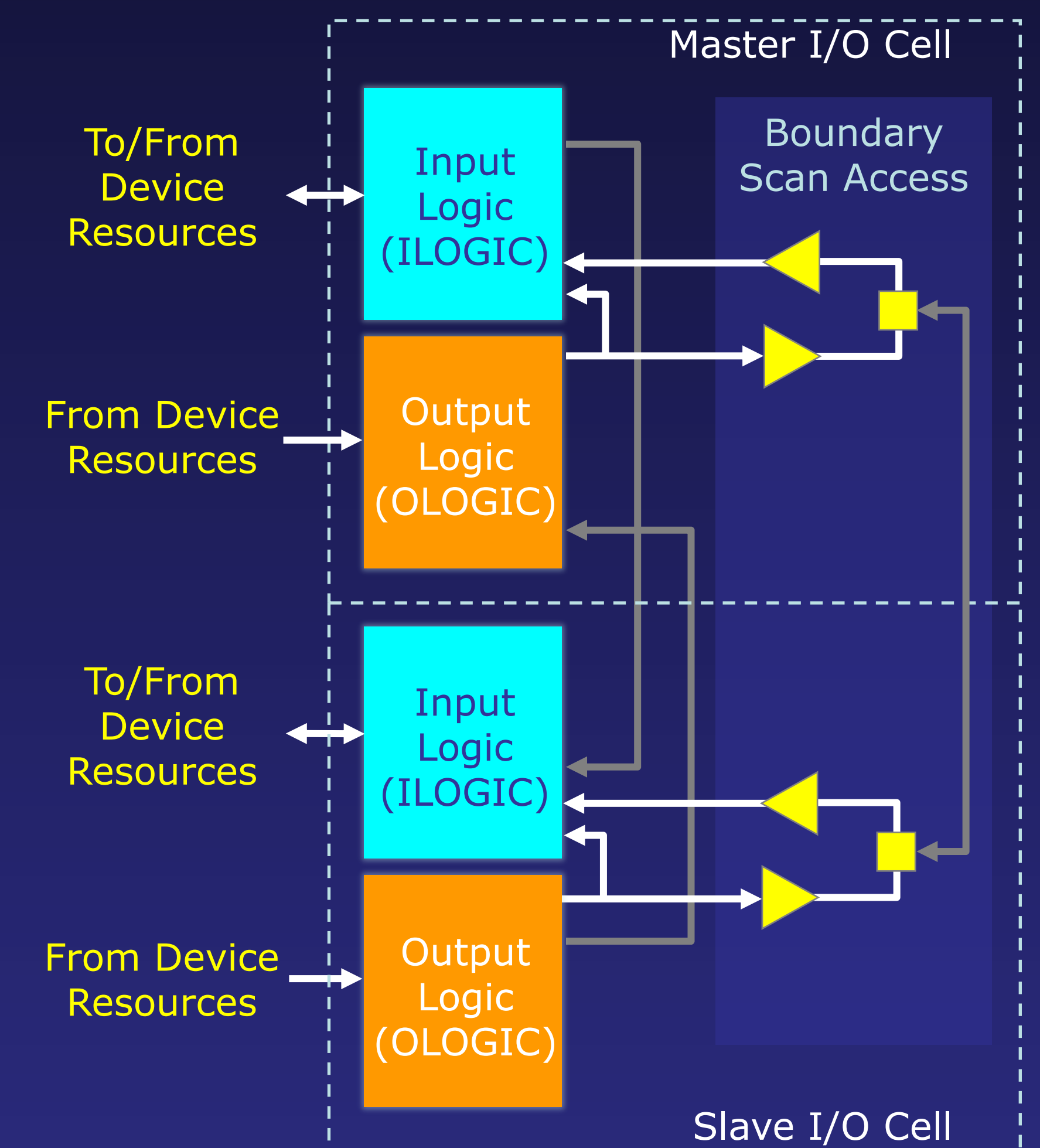
Typical FPGA

## Input/Output Buffer BIST

- Configure bi-directional buffers
- Test patterns are applied to the output buffer and return via the input buffer to ORAs
- One 2-bit counter TPG is configured in a CLB for each I/O buffer under test
- Up-counter applies patterns to slave cell I/O buffer, Down-counter to master cell
- This technique supplies complementary values to the two buffers for testing differential I/O standards
- Most I/O standards support bi-directional buffer operation

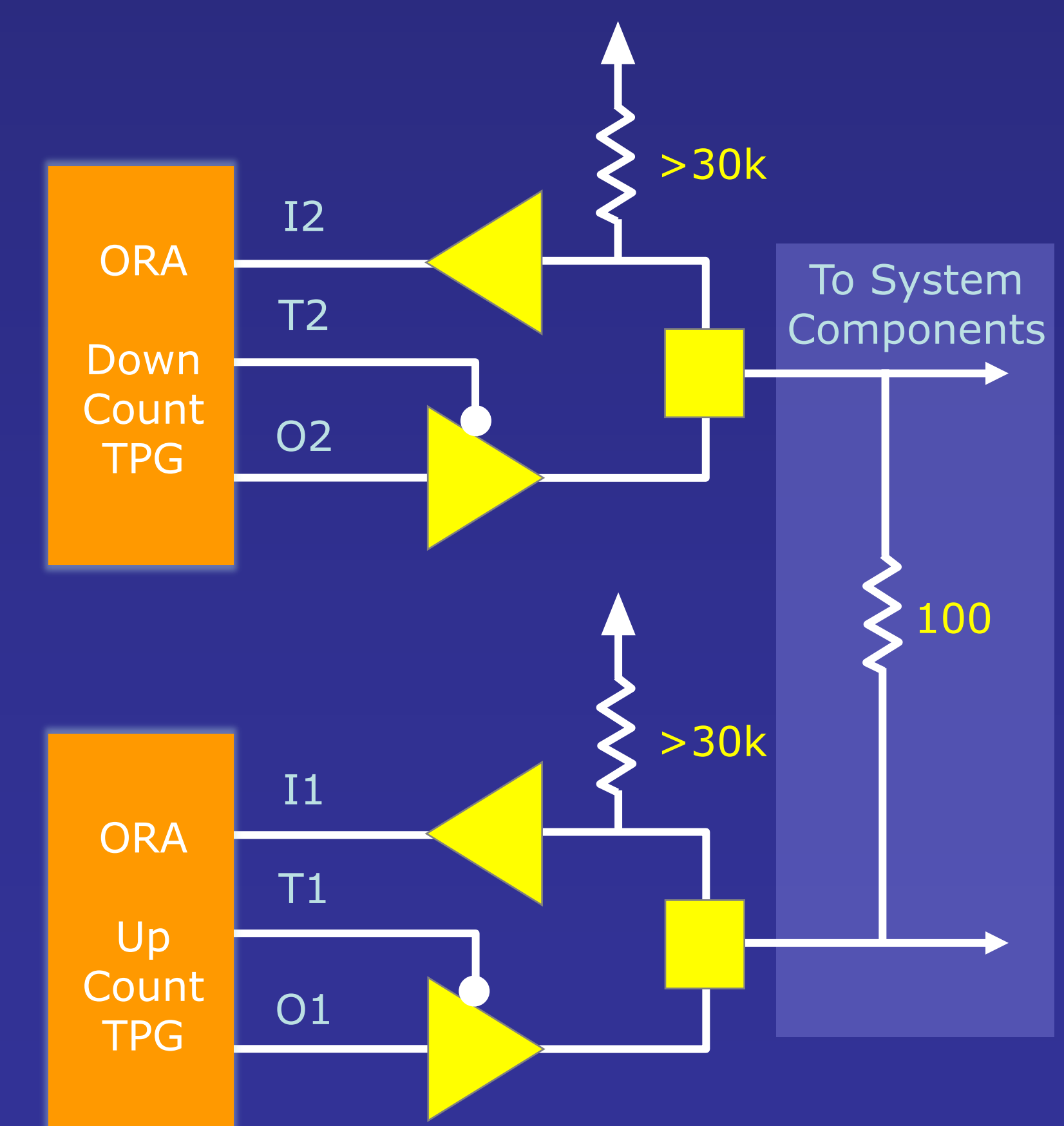
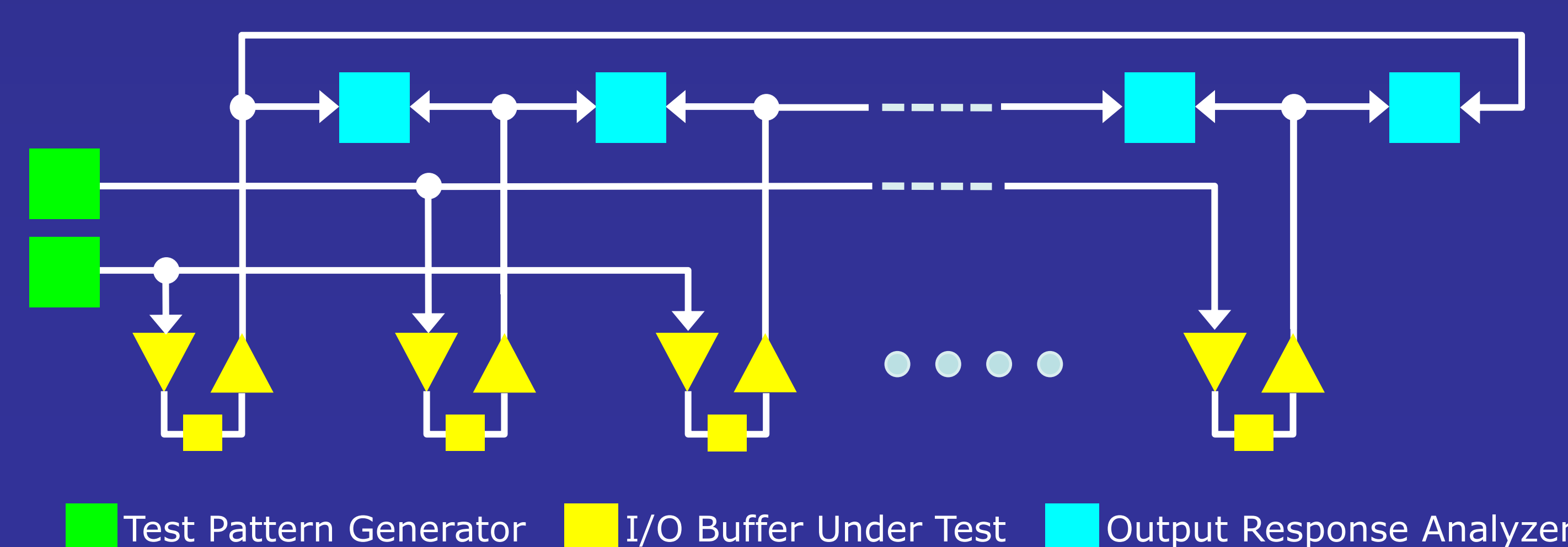
### In-System Implementation Results

- Test configurations are system dependent
- Must configure I/O buffers in the system-mode of operation during test and with compatible I/O standards in each I/O bank
- Connecting digital system components should be tri-stated
- Connecting passive components (LEDs, termination resistors, etc.) can cause failure indication



Virtex-4 Input/Output Tile

## BIST Architecture



I/O Buffer BIST Approach