BENCHMARK CIRCUITS FOR ANALOG AND MIXED-SIGNAL TESTING

Ramakanth Kondagunturi, Eugene Bradley, Kristi Maggard, and Charles Stroud

Dept. of Electrical Engineering
University of Kentucky

***Abstract*:** This paper proposes a standard set of fault models and establishes acceptable component variations for a new set of benchmark circuits used to evaluate analog and mixed-signal testing techniques. [1]

1. INTRODUCTION

The growing need of analog electronics in communication, multimedia and information technology industries has called for the development of analog and mixed-signal integrated circuits with both analog and digital circuits on the same chip. To improve testing capabilities, the IEEE mixed-signal testing committee has been developing a set of benchmark circuits to serve as a reference for performance, comparison of results in fault modeling, testing and other related areas. This set of analog and mixed-signal benchmark circuits was presented at the 1997 IEEE International Test Conference in [1] and are referred to as the ITC'97 mixed-signal benchmark circuits. Additional information regarding these benchmark circuits, including SPICE source files, have been made available on the IEEE mixed-signal benchmark circuit home page (at *www.ee.washington.edu/mad/benchmarks/benchmarks.html*). Our experience with these benchmark circuits in [2] and [3] has shown that the fault models for these circuits, along with a standard list of faults to be simulated, and the range of acceptable component variations were not specified. In addition, other problems were encountered when using the circuits.

In this paper, we propose fault models for the ITC'97 benchmark circuits as well as a standard set of faults and establish the ranges of acceptable component variations for these circuits. Some of the ITC'97 benchmark circuits are omitted due to insufficient model information on the IEEE mixed-signal benchmark circuit home page and in [1]. The omitted benchmark circuit have been replaced and the database has been extended with other circuits from various sources. We begin with an overview of the ITC'97 mixed-signal benchmark circuits in Section 2 and a discussion of the problem encountered with their use. In Section 3 we present the proposed new set of benchmark circuits. The fault model descriptions for the components are described in Section 4. Section 5 gives overview of the simulation method used to establish the component parameter ranges. An example benchmark circuit with brief description, circuit schematic, nominal component values, frequency response of the circuit with out and with variations, set of acceptable parameter variations and soft faults is given in Section 6. Summary and conclusions are presented in Section 7.

2. ITC'97 BENCHMARK CIRCUITS

The ITC'97 benchmark circuits [1] include an operational amplifier, continuous-time state-variable filter (CT filter), a leapfrog filter, digital-to-analog converter, analog-to-digital converter, sixth order band-pass fully-differential filter and a charge-pumped phase lock loop. These circuits are commonly used components in analog and mixed signal circuit design and are intended to be used for comparison of different testing methodologies. However, fault model information including a list of standard faults to be simulated was not presented in [1]. Additional information (such as SPICE source files) for some of the circuits were not available on the IEEE Mixed signal benchmark circuit home page. Therefore, these circuits were discarded in our work as sufficient model information could not be found.

An other difficulty with the ITC'97 circuits is the schematics and spice files do not exactly represent each other for some circuits. For example, the operational amplifier schematic present in [1] illustrates a design with 8 MOSFETs while the Hspice netlist shows a design with 9 MOSFETs. As the operational amplifier is used in the Continuous-time sate-variable filter, we simulated both designs using the both Op Amp models and found that Hspice produced the same outputs for all low-pass, band-pass and high-pass modes. Therefore, we have chosen the model corresponding to the circuit schematic presented in [1]. In another example, there are two different component values specified for the same resistor in the Continuous-time state-variable filter in [1]. Finally, the Hspice source file for

[1] Effort sponsored by Air Force Research Laboratory, Rome Research Site, Air Force Material Command, USAF, Rome, NY, under agreement number F30602-97-1-0042. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright annotation thereon.
0-7803-5237-8/99/$10.00 ©1999 IEEE

Leapfrog filter is modeled with 13 resistors, but circuit schematic shows only 12 resistors.

Analog components are expected to vary in their parameter values as a result of manufacturing tolerances, voltage, temperature, etc. These variations in component values will cause variation in the output response of the analog circuit to test waveforms. In turn, these variations in output response must be considered in testing to determine whether a fault has been detected or not. But none of the ITC'97 benchmark circuits have tolerances associated with their component values. Similarly, a set of benchmark circuits should have a standard set of faults and fault models so that comparison between testing techniques can be accurate. Such a standard set of fault models and fault sets for the ITC'97 benchmark circuits were not presented in [1]. Therefore, there is a need to have a new set of benchmark circuits with fault models and acceptable component variations specified.

3. Proposed New Set of Benchmark Circuits

The proposed new set of benchmark circuits consists of some of the circuits taken from ITC'97 benchmark circuits along with others from different sources like Statistical Fault Analyzer (SFA) [5][6]. These circuits are listed in Table 1 along with their source and the number of components (Rs, Cs, BJTs, and MOSFETs) and number of operational amplifiers that constitute the benchmark circuit.

Table 1: List of new benchmark circuits

Name of the circuit	Source	Number of components
Operational amplifier 1	ITC'97 [1]	11
CT filter	ITC'97 [1]	9 & 3 opamps
Operational amplifier 2	ITC'97 [1]	10
Leapfrog filter	ITC'97 [1]	17 & 6 opamps
Digital to analog conv.	ITC'97 [1]	34 & 1 opamp
Differential amplifier	SFA [5][6]	9
Comparator	SFA [5][6]	3 & 1 opamp
Single stage amplifier	SFA [5][6]	6
Elliptical amplifier	SFA [5][6]	22 & 3 opamps
Low-pass filter	Lucent	4 & 1 opamp

4. Fault Models

Fault models for analog and mixed signal circuits can be classified into two categories: catastrophic faults (sometimes called hard faults) and parametric faults (sometimes called soft faults). A catastrophic fault model is analogous to the stuck-at fault model in the digital domain in that the terminals of the component can be stuck-open or stuck-short. Parametric faults, on the other hand, are deviations of component parameters that result in performance out of acceptable limits. Parametric faults can be simulated as a variation of a component parameter which is out of specified tolerance limits. As will be discussed in Section 5, we establish acceptable component parameter variations using a normal distribution and specify the 1-σ value (expecting the acceptable variation to be up to 3-σ). Therefore we specify parametric faults at the +/- 6-σ values for high and low parametric fault values, respectively. The catastrophic fault models for individual components are described below.

Stuck-open faults are hard faults in which the component terminals are out of contact with the rest of the circuit creating a high resistance at the incident of fault in the circuit. These faults can be simulated by adding a high resistance in series (Rs=100megΩ) with the component to be faulted. A stuck-short fault, on the other hand, is a short between terminals of the component (effectively shorting out the component from the circuit). This type of fault can be emulated by connecting a small resistor in parallel (Rs=1Ω) with the component. Stuck-open and stuck-short faults can be emulated in a resistor or capacitor as illustrated in Figure 1. A MOSFET stuck-on and stuck-off fault can be emulated using this the stuck-open and stuck-short fault model as shown in Figure 1. For the fault-free case Rs=1Ω and Rp=100megΩ.

Another fault model is used for bipolar junction transistors (BJTs). The BJT can have 3 stuck-open faults (at the base, collector, and emitter terminals) 3 stuck-short faults (between base-collector, base-emitter, and collector-emitter). These stuck-open and stuck-short faults are emulated in the same manner using 3 series resistors R_b, R_c, and R_e, for the stuck-open fault (like Rs above) and 3 parallel resistors R_{bc}, R_{be} and R_{ce} (like Rp above), as shown in the Figure 1. In addition, the BJT has two soft faults for the value of β.

With this standard set of faults models we also obtain a standard set of faults. The total number of hard faults in an analog circuit is:

$$N_{HF} = 2(R+C+M)+ 6B \qquad \text{Equation (1)}$$

where R= number of resistors, C= number of capacitors, M= number of MOSFETs and B = number of BJTs in the given circuit. The number of soft faults is:

$$N_{SF} = 2(R+C)+ 2B \qquad \text{Equation (2)}$$

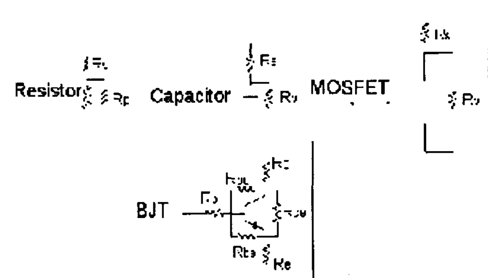

Figure 1. Hard Fault Models

5. Simulation Method

A circuit should be designed to meet the tolerance associated with the specific requirement. Due to the very nature of the manufacturing process and working environment of the designed circuit, the value of the parameters often change. These variations are acceptable as long as circuit response is within specified limits. A known range of acceptable values for a circuit component parameter is necessary to establish the fault-free behavior for a given circuit, which can then be used to detect a fault. To analyze the effects of circuit component parameter variations on the behavior of a circuit, Mote-Carlo analysis is performed.

Monte-Carlo analysis uses a random number generator to generate different kinds of functions like normal and uniform distributions. The normal distribution was chosen to generate statistical variation of component values in order to specify the amount of acceptable variation on each component using standard deviation or 1σ. This specification, in turn, assumes the component will vary up to 3σ yet the analog circuit will continue to operate within the system specification. We chose as a default system specification, a maximum deviation in the gain and phase response of the circuit to be within 10% of the gain and phase response of the circuit when using nominal component values.

In order to facilitate comparison of results like fault coverage through different testing methods for the parametric faults, we propose to use standard soft faults. The 6σ point on the either side of the nominal value is defined as a standard parametric fault or soft fault for each component, where 1σ point represents the amount of acceptable variation in Gaussian distribution. The representation of soft faults is shown in figure 3

6. Example Benchmark Circuit

In this section we illustrate the information contained in our new benchmark circuit database which can be found at www.engr.uky.edu/EE/Stroud/anabckts.html. For each benchmark circuit we include the following information:

1. Schematic diagram
2. Nominal component values
3. Frequency response (gain and phase) using nominal component values
4. Acceptable component parameter variations
5. Frequency response (gain and phase) using acceptable component variations
6. Catastrophic (hard) fault list
7. Parametric (soft) fault list
8. Hspice/SPICE netlist source file with fault models (with fault-free values) included

We will use operational amplifier 1 (Op Amp 1) from Table 1 as an example circuit to show the format of the information listed above. The schematic diagram of the CMOS two stage operational amplifier is shown in Figure 2 and the nominal component values for each component in Op Amp 1 are listed in Table 2. The frequency response of the circuit using the nominal component values is given in Figure 3 for both gain and phase. It is important to note that the operational amplifier was simulated in Hspice with fault models for its component included and that the fault-free values were used for the nominal frequency response simulation. The unity gain bandwidth and open-loop gain are 16.5MHz and 77.5 db respectively.

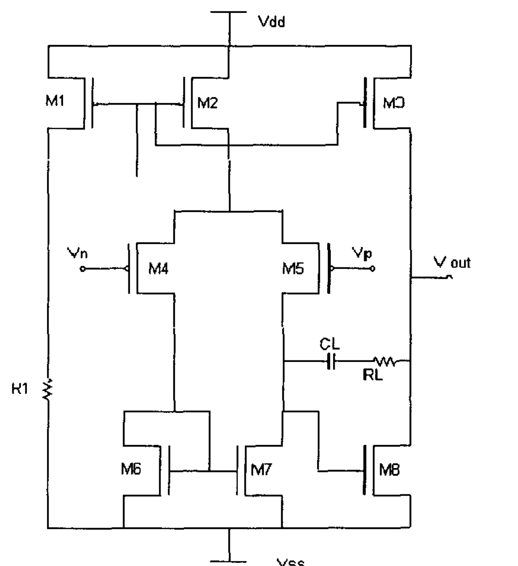

Figure 2: Schematic Diagram.

Table 2: Component table with nominal values

Component: number of each	Nominal Value
MOSFETs: 8	M1-M8
Capacitor: 1	CL=1.27pF
Resistors: 2	R1=110KΩ, RL=8.75KΩ

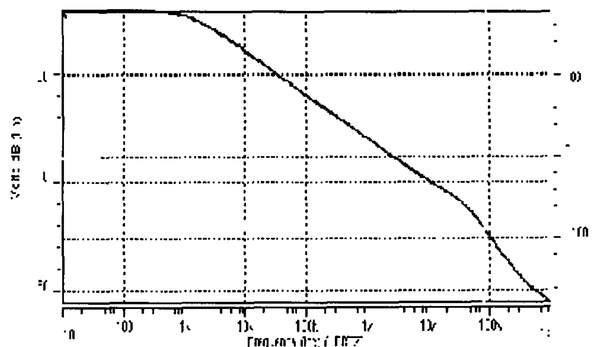

Figure 3: Frequency response with nominal components

The information presented thus far was obtained from the benchmark circuit source (with the exception of the fault models incorporated in the Hspice/SPICE netlist source file.

Having described the method for modeling the hard and soft faults for the benchmark circuit, we summarize the fault data presented in our benchmark circuit database. The set of catastrophic (or hard) faults for Op Amp 1 are summarized in Table 3. The total number of hard faults according to Equation 1 is 22 for Op Amp 1. Similarly the soft faults are summarized in Table 4 where the total number of faults given by Equation 2 is 6.

Table 3: Hard faults and number of faults

Component	Faults	No. of faults
M1-M8	Stuck-open/stuck-short	2x8=16
R1,RL	Stuck-open/stuck-short	2x2=4
CL	Stuck-open/stuck-short	1x2=2

Table 4: Soft faults component values

Component	Nominal value	-6σ	$+6\sigma$
R1	110KΩ	70.4KΩ	149.6Ω
RL	8.75KΩ	5.6KΩ	11.9KΩ
CL	1.27pF	0.3556pF	2.1844pF

The acceptable component parameter variations that were established via the Monte-Carlo analysis described in the previous section are summarized for Op Amp 1 in Table 5. Although each component variation is specified at the 1σ point in the table, we emphasize that the component can vary in value by as much as 3σ from the nominal value. With the specified component variations, the gain and phase response of the analog circuit will remain within 10% of the gain and phase response of the circuit using only nominal component values. This frequency response with component variation is shown in Figure 4 for Op Amp 1.

Table 5: Acceptable component parameter variations

Component	Nominal value	1σ point value
R1	110KΩ	6.6KΩ
RL	8.75KΩ	525Ω
CL	1.27pF	0.1524pF

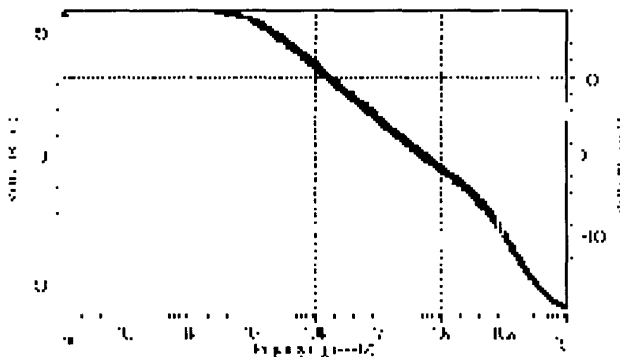

Figure 4: Frequency response with component variation

7. Summary and Conclusions

A standard set of faults and fault models for analog and mixed-signal benchmark circuits have been presented and proposed that can be applied to any analog circuit. This set of faults and fault models includes hard and soft faults for the evaluation and comparison of different analog and mixed-signal testing approaches. The set of analog and mixed-signal testing benchmark circuits originally described in [1] has modified and expanded with new benchmark circuits from other sources. Acceptable component parameter variations is established for each benchmark circuit which ensures no more than a 10% variation in the analog circuit gain and phase frequency response. A web site (www.engr.uky.edu/EE/Stroud/anabckts.html) was prepared to make this information readily available on-line to the public and to other researchers.

Acknowledgements

The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the Air Force Research Laboratory or the U.S. Government.

References

[1] B. Kaminska, K. Arabi, I. Bell, P. Goteti, J.L. Heurtas, B. Kim, A. Rueda, and M. Soma "Analog and Mixed-Signal Benchmark Circuits - First Release", IEEE International Test Conference, Washington DC, November 1997.

[2] C. Stroud, P. Karunaratna, and E. Bradley, "Digital Components for Built-In Self-Test of Analog Circuits", Proc. IEEE International Application Specific Integrated Circuits Conf., pp. 47-51, 1997.

[3] K. Maggard, P. Karunaratna, C. Stroud, "Built-In Self-Test for Analog Circuits in Mixed-Signal Systems", Proc. IEEE Southeast Regional Conf., 1999.

[4] W.G. Jung, IC Op-Amp Cookbook, Howard W. Sams & Co., Indianapolis, 1974.

[5] E. Ratazzi, "Fault Coverage Measurement for Analog Circuits", Proc. IEEE Custom Integrated Circuits Conf., pp. 17.2.1-4, 1992.

[6] B. Epstein, M. Czigler and S. Miller, "Fault Detection and Classification in Linear Integrated Circuits: An Application of Discrimination Analysis and Hypothesis Testing", IEEE Trans. on CAD, Vol. 12, No. 1, pp. 102-113, 1993.