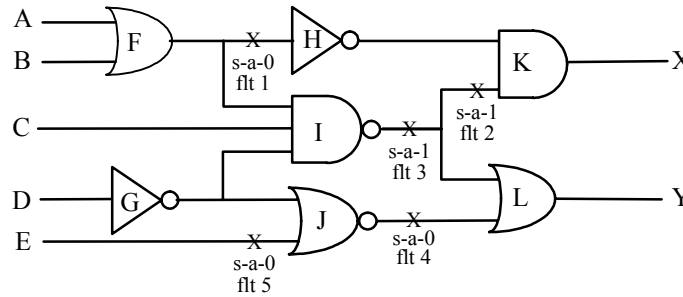


**Chapter 1. An Overview of Built-In Self-Test**

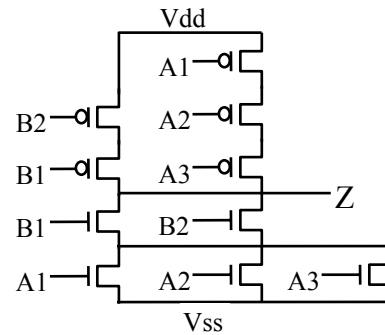
1. Excluding the circuit under test, what are the four basic components of BIST and what function does each component perform?
2. Which two BIST components are necessary for system-level testing and why?

**Chapter 2. Fault Models, Detection, and Simulation**

1. Given the following gate-level circuit diagram:



- a. Does the circuit contain reconvergent fanout?
  - b. How many fault sites are in the circuits?
  - c. What is the total number of uncollapsed single stuck-at gate-level faults?
  - d. What is the total number of collapsed single stuck-at gate-level faults?
  - e. What is the total number of faulty circuits considered in the multiple stuck-at gate-level fault model?
  - f. Give the complete set of collapsed single stuck-at gate-level faults.
  - g. For each of the five single stuck-at gate-level faults shown in the circuit, use path sensitization to determine whether the fault is detectable or not. If the fault is detectable, give a test pattern (indicating input ordering) that will detect the fault and indicate the output(s) at which the fault will be detected.
2. Given the following transistor-level circuit diagram:
    - a. How many fault sites are in the circuit?
    - b. What is the total number of uncollapsed single stuck-at transistor-level faults?
    - c. What is the total number of collapsed single stuck-at transistor-level faults?



3. What type of transistor-level faults are detected by  $I_{DDQ}$  testing?
4. Assume that a circuit has 400 faults and that for a given set of test vectors, 350 faults are detected, 50 faults are not detected and 30 faults are potentially detected. Calculate the fault coverage.

**Chapter 3. Design for Testability**

1. Assume a sequential circuit with 100 flip-flops plus 1000 additional logic gates, 20 primary inputs, and 15 primary outputs.

- a. Determine the area overhead in terms of gates for a full scan design implementation assuming a multiplexer is 3 gates and a flip-flop is 9 gates.
- b. Determine the number of clock cycles needed for scan testing if the combinational logic portion of the circuit requires 50 test vectors.

#### Chapter 4. Test Pattern Generation

1. Given the polynomial  $P(x)=x^4+x^2+x+1$ :
  - a. Design an external feedback LSFR with characteristic polynomial  $P(x)$ .
  - b. Starting this LFSR in the all 1s state, determine the sequence produced.
  - c. Is this a maximal length LFSR?
  - d. Is the characteristic polynomial primitive?
2. Design a register bit for CA rule 175 and draw the logic diagram labeling all I/O?
3. Assume a 4-bit CA register with null boundary conditions that uses alternating rules of 90 and 150:
  - a. Draw a gate and flip-flop level diagram of the complete register.
  - b. Determine the sequence of test patterns produced by this register once it has been preset to the all 1s state.

#### Chapter 5. Output Response Analysis

1. For an internal feedback Signature Analysis Register with characteristic polynomial  $P(x)=x^6+x^2+1$ :
  - a. Draw a logic diagram for the complete register.
  - b. Determine the resultant signature that would be obtained for the following serial sequence of output responses produced by a known good CUT assuming the SAR is initialized to the all 0s state. Give the binary value of the resultant signature as it would be contained in the SAR in your logic diagram above.
 
$$101001010010 \leftarrow \text{time}$$
  - c. Give the error polynomial assuming the following serial sequence of output responses produced by a faulty CUT. Would this error polynomial lead to signature aliasing?
 
$$011001110010 \leftarrow \text{time}$$
2. What is the minimum number of test vectors needed to test an  $N$ -bit comparator? Give the set of test vectors for  $N=4$ . Assume combinational logic only – no latch is included.