# 2011 IEEE NORTH ATLANTIC TEST WORKSHOP

## MAY 11-13, UNIVERSITY INN AND CONFERENCE CENTER, LOWELL, MA

**The IEEE North Atlantic Test Workshop** provides a forum for discussions on the latest issues relating to high quality, economical, and efficient testing methodologies and designs. With the increasing complexity and density in both design and test of integrated circuits and systems, the **20th NATW** features the theme: *"Drive to Nanoscale"* and a **Panel** dedicated to *the next 20 years of test*. This year's NATW includes 20 papers from 7 different companies and 13 different universities, including 13 student papers competing for the **Jake Karrfalt Best Student Paper Award**. In addition, the workshop includes a Keynote Address on chips with 10's of billions of transistors, a 1st Invited Address on the impact of increasing circuit complexity on fault management, and a 2nd Keynote Address on analog test. The 2011 workshop is held at the University Inn and Conference Center at the University of Massachusetts, Lowell, MA and is sponsored, in part, by the Green Mountain Section of IEEE. It is organized in cooperation with TTTC and the IEEE Boston Section. NATW corporate and academic supporters for 2011 include Mentor Graphics, SynTest Technologies, Cadence, Amkor, AdamsIP, Maxim, the Wireless Engineering Research and Education Center at Auburn University, and the Vermont chapter of the IEEE Solid State Circuits Society.

| Time | Event |
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| **Wednesday, May 11** | |
| **6:30 - 7:00 pm** | **Welcome Reception and Registration** |
| **7:00 – 8:00 pm** | **Invited Tutorial:** "Statistical Testing, Benefits and Limitations". Jeff Roehr, MediaTek |
| **8:00 - 9:00 pm** | **Panel Session:** "The Next 20 Years of Test". Panel Chair: Gene Atwood (IBM)<br>**Panelists**: Nematollah Bidokhti (Cisco), Carl Moore (Maxim Integrated Products), Brion Keller (Cadence), and Gary W. Maier (IBM) |
| **Thursday, May 12** | |
| **7:00 - 8:00 am** | **Breakfast** |
| **8:00 - 8:15 am** | **Opening Remarks:** Martin Margala, *General Chair* |
| **8:15 - 9:00 am**<br>*Introduction by Martin Margala, Program Co-Chair* | **Keynote Address:** "Scaling into 15 nm, 11 nm, and Beyond: Moving Toward Chips With 10's of Billions of Transistors" by Dr. Ghavam Shahidi (IBM)<br>**Abstract:** Moore's Law and the scaling of microelectronics is expected to extend to 11 nm and most probably beyond. The key challenges are lithography, and fitting the device and the interconnect into a shrinking footprint. In this talk, we will discuss some of the requirements for the device, interconnect, and power density challenges, as we scale to 11 nm. It is expected that even in the presence of power challenges scaling will continue. That in turn will enable chips with 10's of billions of transistors (especially when coupled with 3D). Such high level of device count poses its own challenges in design and test. |
| **9:00 - 9:45 am**<br>*Introduction by Jennifer Dworak, Program Co-Chair* | **Invited Address:** "Robust Design & Dynamic System Fault Management" by Nematollah Bidokhti (Cisco)<br>**Abstract:** As technology advances, system design and complexity increases a well. This is due to a number of reasons; but improvement in transistor size and integrated circuit performance has had the most impact. A number of industries has enjoyed a phenomenal growth and success based on new technologies and capabilities. This does not come for free. The growth and advances in technology has brought with it a set of challenges that need to be addressed in product designs. For example:<br>· Understanding and mitigating the impact of faults in a complex system design<br>· What types of policies should be created to handle faults?<br>· How should device variation and aging be addressed?<br>· Which element of a system design is responsible for fault management?<br>· How many new types of failure modes a system will experience?<br>· What are the new environmental challenges for new advanced devices? |
| **9:45 - 10:10 am** | **Coffee Break / Reception** |
| **10:10 - 11:30 am** | **Student Session 1: Design for Test, Reliability, and Trust,** Session Chair: TBD |
| | 1.1 Design and Analysis of Ring Oscillator based Design-for-Trust technique. J. Rajendran, V. Jyothi, R. Karri, O. Sinanoglu (Polytechnic Institute of New York University and New York University, Abu Dhabi)<br>1.2 Variation Tolerance Mapping for Nano-PLA Architectures. M. Zamani and M. Tahoori (Northeastern Univ. and Karlsruhe Institute of Technology)<br>1.3 Noise-Immune CMOS Circuits for Sub-Threshold Operation Using Schmitt-Trigger Logic. M. Donato, K. Nepal, R. I. Bahar, W. Patterson, A. Zaslavsky, and J. Mundy (Brown University)<br>1.4 Hardware State Monitors for Estimating Fault Detection Counts. Y. Shi, K. Kaewtip, W.-C. Hu, and J. Dworak (Brown University, UCLA, MStar Semiconductor, and Southern Methodist University) |
| **11:30 - 12:00 pm** | **Break** |
| **12:00 - 1:00 pm** | **Lunch** |

| Time | Program |
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| **1:00 - 2:00 pm** | **Student Session 2: Analog Test,** Session Chair: TBD |
| | 2.1 LNA Test: A Polynomial Coefficient Approach. S. Sindia, V. Agrawal, and F. F. Dai (Auburn Univ.)<br>2.2 Time-Based Parametric Built-in Test for Analog/Mixed-Signal Circuits. K. Kulovic and M. Margala (U. Mass. - Lowell)<br>2.3 An Analytical Model for All-Digital PLL Phase Noise Characterization. B. Jiang, T. Xia (Univ. of Vermont) |
| **2:00 – 2:15 pm** | **Break** |
| **2:15 - 3:15 pm** | **Student Session 3: Aging and Wearout** Session Chair: TBD |
| | 3.1 A Framework for Fast and Accurate Critical-Reliability Paths Identification. J. Chen, S. Wang, N. Bidokhti, and M. Tehranipoor (Univ. of Connecticut and Cisco)<br>3.2 Experimental Analysis for Aging in Integrated Circuits. N. R. Kayam, S. Wang, L. Winemberg and M. Tehranipoor. (Univ. of Connecticut and Freescale)<br>3.3 NBTI-Aware Data Allocation Strategies for Scratchpad Memory Based Embedded Systems. C. Ferri, D. Papagiannopoulou, R. I. Bahar, A. Calimera (Brown University & Politecnico di Torino) |
| **3:15 - 3:30 pm** | **Break** |
| **3:30 – 4:10 pm** | **Student Session 4: Test Coverage and Diagnosis,** Session Chair: TBD |
| | 4.1 Diagnostic Test Generation and Fault Simulation Algorithms for Transition Faults. Y. Zhang and V. Agrawal (Auburn University)<br>4.2 Increasing SDD Coverage Without Increasing Pattern Count. F. Bao, K. Peng, K. Chakrabarty, and M. Tehranipoor (University of Connecticut, Freescale, and Duke University) |
| **4:10pm – 6 pm** | **Break** |
| **6 pm – 8 pm** | **Banquet and Best Student Paper Award** |
| **Friday, May 13** | |
| **7:30 - 8:00 am** | **Breakfast** |
| **8:00 - 8:45 am** | **Friday Keynote Address:** "Analog Integrated Circuit Test: Where we have come from...and where we need to go" by Carl Moore (Maxim Integrated Products)<br>**Abstract:** Analog Integrated Circuit test has always had many challenges. As the technology shrinks, and the complexity grows, the challenges become even more important to solve. The Handheld Power consumer market demands higher levels of integration, and requires fast development times, lower cost, and high quality. The importance of test has grown significantly. We will look at some of the areas of Analog Power SoC test, highlight the challenges, and discuss areas where there are still major advances needed in Analog test |
| **8:45 – 8:55 am** | **Break** |
| **8:55 - 10:10 am** | **Session 5: Special Session on Testing at IBM,** Session Chair: Pascal Nsame |
| **10:10 - 10:20 am** | **Break** |
| **10:20 - 12:00 pm** | **Session 6: Functional and Structural Test and Characterization** Session Chair: TBD |
| | 6.1 Trace, Debug, Mask, Deploy: Accuracy & Efficiency in Poulson Scanout Methodology, Michael Lohmiller and Justin Fidler (Intel)<br>6.2 A Fast Boolean Solver for choosing load/store addresses to test a CPU uncore, J. Grodstein, N. Karim, M. McGrath, S. Murphy, and R. Nettleton (Intel)<br>6.3 Factors Affecting tATPG Pattern Frequency. E. R. Skeels and P.Pant (Intel)<br>6.4 Virtual Circuit Model for Low Power Scan Testing in Linear Decompressor-based Compression Environment. Z. Chen, J. Li, D. Xiang, and Y. Huang (Tsinghua University and Mentor Graphics) |
| **12:00 - 1:00 pm** | **Lunch and Program Committee Meeting** |
| **1:00 - 2:15 pm** | **Session 7: Advances in DFT and Diagnosis,** Session Chair: TBD |
| | 7.1 A Case Study of Compound Hold Time Faults Caused by Spot Delay Defects at Clock Tree. Y. Huang, W.-T. Cheng, T.-P. Tai, L. Lai, R. Guo, F. M. Kuo, Y.-S. Chen (Mentor Graphics and TSMC)<br>7.2 The Embedded ATE. A. Crouch and S. Hack (ASSET-InterTech)<br>7.3 Automation of DfT Insertion and Interconnect Test Generation for 3D Stacked Dies. S. Deutsch, V. Chickermane, B. Keller, M. Konijnenburg, and E. J. Marinissen (Cadence and IMEC) |
| **2:15-2:20 pm** | **Closing Remarks**, Martin Margala |