Bi-directional signals in IEEE P1500 Standard

By:
Nitin Yogi
Why is testing important?

- Need to ascertain that manufactured chips work.
- Testing saves cost of replacement and compensation for faulty chips.
- Testing enables detection of design errors.
System on Chip (SoC)

System on Chip (SoC) is a chip which holds all the necessary hardware to make a complete electronic system.

SoCs comprise on-chip memory, processors, peripheral devices, I/O logic control and other components each referred to as cores.
SoC Example

Advantech’s EVA-X1610C: 16-bit, 75 MHz RISC microprocessor with Ethernet and RS-232 connectivity

![SoC Example Diagram]
SoC testing

- SoC design has primarily evolved around core design and core reuse.
- Usage of pre-designed re-usable embedded cores is fast becoming a popular practice in industry for SoC design.
- SoC testing is also based on core level testing and core test reuse.
- Design for Testability (DFT) methodology suits well to core-level testing of SoCs
Proposed DFT based SoC test standard that facilitates embedded core testing and core test reuse

Standardizes test information transfer model and on-chip test access hardware.

– The Core Test Language (CTL) is the information transfer model of the P1500.
– The Scalable Test Access Architecture comprises the hardware guidelines.
Scalable Core Test Architecture

- The Scalable Core Test Architecture comprises:
  - Source and Sink for test stimuli and responses.
  - Test Access Mechanism (TAM)
  - Wrapper

- The source and sink for test stimuli are provided by the testing equipment.
- TAMs are mechanisms used to transfer test vectors and responses to and from the core, respectively.
- Wrappers exists around each core to connect TAMs to the cores.
Scalable Core Test Architecture (System-level overview)
Scalable Core Test Architecture (SoC test view)
Test Access Mechanisms (TAMs)

TAMs are characterized by:

- TAM width: determines the test data transport bandwidth.
- TAM length: the physical distance of the TAM.
Wrapper

- Wrapper connects the TAM to the core and thus determines the normal or testing mode of the core.
- One wrapper exists for each core and totally encapsulates the core.
The Wrapper Serial Input and Output are serial interfaces to the wrapper.

The Wrapper Bypass Register routes data flowing from WSI to WSO, to bypass the core.
Wrapper Instruction Register (WIR)

- WIR loads and executes test instructions.
- WIR is a SHIFT/UPDATE register, similar to JTAG’s instruction register.
- WIR configures the operation of the wrapper, according to the instruction shifted into it.
- WIR circuitry decodes loaded instructions and provides individual control signals to WBR, WBY or Data registers.
Wrapper Interface Port

WIP comprises of control signals applied to the WIR and determine the functioning of the wrapper.

- WRSTN : Asynchronous Wrapper Reset
- WRCK : Wrapper Clock
- SelectWIR : Control signal to select between Wrapper Instruction Register and Wrapper Data Registers
- ShiftWR : Shift control Signal
- CaptureWR : Capture control signal
- UpdateWR : Update control signal
Wrapper Boundary Register (WBR)

- WBR consists of boundary scan cells (BSCs) connected in series.
- One BSC per core terminal.
- Two types of BSCs defined:
  - BSC for input terminal
  - BSC for output terminal
- IEEE P1500 does not support bidirectional terminals, hence no bidirectional BSC is defined.
# P1500 Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Mode</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WS_BYPASS</td>
<td>Normal + Serial Bypass</td>
<td>Mandatory</td>
<td>Wrapper allows functional mode, WSI-WSO connected through WBY</td>
</tr>
<tr>
<td>WS_EXTEST</td>
<td>Serial Extst</td>
<td>Optional</td>
<td>External core testing using serial interface</td>
</tr>
<tr>
<td>WP_EXTEST</td>
<td>Parallel Extst</td>
<td>Optional</td>
<td>External core testing using parallel interface</td>
</tr>
<tr>
<td>WH_EXTEST</td>
<td>Hybrid Extst</td>
<td>Optional</td>
<td>External core testing using hybrid interface</td>
</tr>
<tr>
<td>WS_INTEST_RING</td>
<td>Serial Intst</td>
<td>At least one of them is mandatory</td>
<td>Internal core testing using serial interface</td>
</tr>
<tr>
<td>WS_INTEST_SCAN</td>
<td>Serial Intst</td>
<td></td>
<td>Internal core testing using serial interface with internal core scan chains included</td>
</tr>
<tr>
<td>WP_INTEST_RING</td>
<td>Parallel Intst</td>
<td></td>
<td>Internal core testing using parallel interface</td>
</tr>
<tr>
<td>WP_INTEST_SCAN</td>
<td>Parallel Intst</td>
<td></td>
<td>Internal core testing using serial interface with internal core scan chains included</td>
</tr>
<tr>
<td>WS_PRELOAD</td>
<td>Serial Preload</td>
<td>Optional</td>
<td>Loads data into dedicated shift path of WBR</td>
</tr>
<tr>
<td>WP_PRELOAD</td>
<td>Parallel Preload</td>
<td>Optional</td>
<td>Loads data into dedicated shift path of WBR</td>
</tr>
<tr>
<td>WS_CLAMP</td>
<td>Other</td>
<td>Optional</td>
<td>Clamps output terminals of WBR to predefined states (Requires PRELOAD)</td>
</tr>
<tr>
<td>WS_SAFEESTATE</td>
<td>Other</td>
<td>Optional</td>
<td>Clamps output terminals of WBR to predefined states (Does not require PRELOAD)</td>
</tr>
</tbody>
</table>
BSC Operation - BYPASS
BSC Operation - EXTEST
BSC Operation - INTEST
BSC Operation – PRELOAD
BSC implementation

Input Boundary Scan Cell

Output Boundary Scan Cell
Core Test Language (CTL)

- CTL is the information transfer model of IEEE P1500
- CTL is an extension to the IEEE 1450 Standard Test Information Language (STIL) standard and is named as P1450.6
- Core providers package CTL code with their cores to make it IEEE P1500 testable.
- CTL information includes:
  - Design Configuration Information
  - Structural Information
  - Test Pattern Information
**CTL Design Configuration Information**

- Describes wrappers
- Describes controls to configure the core for testing the core and the surrounding SoC logic.

### Environment wrapped_core

<table>
<thead>
<tr>
<th>Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>A In; B Out;</td>
</tr>
<tr>
<td>Y In; Z In;</td>
</tr>
<tr>
<td>SE In; BSE In;</td>
</tr>
<tr>
<td>CLK In; BCK In;</td>
</tr>
<tr>
<td>SI In { ScanIn 2; } SO Out { ScanOut 2; }</td>
</tr>
<tr>
<td>BSi In { Scanin 2; } BSO Out { ScanOut 2; }</td>
</tr>
</tbody>
</table>

```plaintext
Environment wrapped_core {  
   CTL myN {  
       TestMode Normal;  
       Internal {  
           Y+Z { DataType TestMode;  
               ActiveState ForceDown; }  
       }  
   }  
   PatternInformation {  
       Pattern P1 {  
           Purpose EstablishMode; }  
   }  
}
```

```plaintext
CTL myE {  
   TestMode External;  
   Internal {  
       Y { DataType TestMode;  
           ActiveState ForceDown; }  
       Z { DataType TestMode;  
           ActiveState ForceUp; }  
   }  
   PatternInformation {  
       Pattern P2 {  
           Purpose EstablishMode; }  
   }  
}
```

---

23
CTL Structural and Test Pattern Information

- **Structural Information**
  - Describes requirements and constraints on the implementation of SoC level interface to the core.

- **Test Pattern Information**
  - Describes inclusion of test data specific to the core, but independent of any particular use of the core.
Core pin types

- Input Pins - dedicated inputs
- Output Pins - dedicated outputs
- Programmable Pins - programmed as either input or output. They remain as programmed until reprogrammed
- Bi-directional Pins - signals can flow either in or out of the core; direction is determined by an internal control signal
Bi-directional pins

- A bi-directional pin has tri-state drivers for transmitting data and a buffer for receiving data.
- Difficult to test in the absence of signal direction knowledge.
Bi-directional pins

- P1500 requires bidirectional signals to be split into input, output and control signals.
- Disadvantage is an increase in SoC routing interconnect overhead and area.
Testing of bidirectional signals (IEEE P1500)
Proposed Test Structure

- Split bi-directional signals inside the wrapper
- Place input, output and control boundary scan cells on the respective signal lines
- Bidirectional control signal from the core controls the direction.
BYPASS in the proposed structure
Bidirectional BSC analysis
BSC structure analysis

Diagram showing the BSC structure analysis with various components labeled with nodes and connections.
Combining input and output BSCs

Input BSC

Output BSC

Bidirectional BSC
Bidirectional BSC analysis
BSC Control Structure
Conventional vs Modified Bidirectional BSC – Transistor Count

Transistor count vs Bus-width for Conventional and Modified Bi-directional BSC

Reduction of more than twice in the number of transistors
### Conventional vs Modified Bidirectional BSC - Delays

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Conventional</th>
<th>Modified</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bypass Delay Ter.1 =&gt; Ter.2</td>
<td>550 ps</td>
<td>730 ps</td>
</tr>
<tr>
<td>Drive Delay BSC reg. =&gt; Ter.</td>
<td>860 ps</td>
<td>930 ps</td>
</tr>
<tr>
<td>Capture Delay Ter. =&gt; BSC reg.</td>
<td>1000 ps</td>
<td>1700 ps</td>
</tr>
</tbody>
</table>
Implementation of P1500 instructions

Three IEEE P1500 instructions are mandatory:

- WS_BYPASS / WS_PRELOAD
- WS_INTEST_RING / WS_INTEST_SCAN
- WS_EXTEST
WS_BYPASS / WS_PRELOAD

The testing structure is disabled, although test vectors can be loaded into the cell registers.
Implementation of WS_BYPASS / WS_PRELOAD instruction

Conventional BSC
Implementation of WS_BYPASS / WS_PRELOAD instruction

Modified BSC
Testing structure is enabled and is assumed to be preloaded with test vectors.

This is an inward facing test directed towards the core to test it.

We need to consider two cases, bidirectional BSC configured as:
- Input BSC
- Output BSC
Implementation of WS_INTEST_RING / WS_INTEST_SCAN instruction

Bidirectional BSC configured as an Input BSC
Conventional BSC
Implementation of WS_INTEST_RING / WS_INTEST_SCAN instruction

Bidirectional BSC configured as an Input BSC

Modified BSC
Implementation of WS_INTEST_RING / WS_INTEST_SCAN instruction

Bidirectional BSC configured as an Output BSC

Conventional BSC
Implementation of WS_INTEST_RING / WS_INTEST_SCAN instruction

Bidirectional BSC configured as an Output BSC

Modified BSC
The testing structure is enabled and assumed to have been preloaded with test vectors.

This is an outward facing test directed towards the interconnects.

We need to consider two cases, bidirectional BSC configured as:
- Input BSC
- Output BSC
Implementation of WS_EXTEST instruction

Bidirectional BSC configured as an Input BSC

Conventional BSC
Implementation of WS_EXTEST instruction

Bidirectional BSC configured as an Input BSC

Modified BSC
Implementation of WS_EXTEST instruction

Bidirectional BSC configured as an Output BSC

Conventional BSC
Implementation of WS_EXTEST instruction

Bidirectional BSC configured as an Output BSC

Modified BSC
Digital switch constructed using CMOS technology, which connects two terminals when activated and disconnects them when deactivated.

Consists of an NMOS and a PMOS transistor
- An NMOS transistor turns ON when logic ‘1’ is applied to its gate terminal.
- A PMOS transistor turns ON when logic ‘0’ is applied to its gate terminal.
Transmission Gate Issues

- Requires both NMOS and PMOS transistors
- Requires use of complementary control signal.
- Leakage current due to non-infinite OFF impedance.
  - Can be reduced by proper scaling of MOS transistors and proper design of the circuits connected to transmission gate.

Major issues:
- serial loading due to finite ON impedance
- absence of inherent driving capability.
Solutions to Transmission Gate low-drive issue.

1. Connect additional circuit to the signal line in parallel with the transmission gate structure:
   - Bus-hold circuit
   - Bidirectional repeater

2. Replace the transmission gate structure so that it provides sufficient drive strength along with the bidirectional switch functionality.
Bus-Hold Circuit

- Provides a defined logic state to floating buses.
- Acts as a bus-hold circuit and a logic restorer and driver circuit, due to the driving inverters.
- The drive delay was found to be 300ps.
Bidirectional repeater circuit

- Combination of positive and negative feedback keeps the output node in high impedance state.
- On signal transition, driver circuit is enabled by positive feedback.
- The delayed negative feedback disables the driver circuit later.
- The drive delay was found to be 250ps.
Buffered Memory Cell

- Consists of two back-to-back inverters with a transmission gate at the output of each inverter.

- The transmission gate reduces the loading of the output inverters.

- Provides required drive for the signal line and acts as a bidirectional switch.
Comparison of signal boosting circuits (driving logic ‘0’)
Comparison of signal boosting circuits (driving logic ‘1’)
## Comparison of signal boosting circuits

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Bus-Hold circuit</th>
<th>Bidirectional Repeater</th>
<th>Buffered Memory Cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transition delay of the signal line under consideration</td>
<td>May affect to some extent, as the bus-hold circuit can load the signal line.</td>
<td>Does not affect, as the bidirectional repeater does not load the signal line.</td>
<td>Transition delay of two inverters and one transmission gate</td>
</tr>
<tr>
<td>Drive Delay</td>
<td>Transition delay of two inverters and one transmission gate. Equal to 300ps*</td>
<td>Transition delay of inverter in positive feedback. Equal to 250ps*</td>
<td>Transition delay of two inverters and one transmission gate. Equal to 440ps*</td>
</tr>
<tr>
<td>Steady State Characteristics</td>
<td>Driver</td>
<td>High-impedance state</td>
<td>Driver</td>
</tr>
<tr>
<td>Transition State Characteristics</td>
<td>Loads the signal line</td>
<td>Driver</td>
<td>Driver</td>
</tr>
<tr>
<td>Bus-contention resistance</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Drive Duration</td>
<td>Continuous except the drive delay</td>
<td>For a duration equal to the gate delay in the negative feedback from the transition point</td>
<td>Continuous</td>
</tr>
<tr>
<td>Drive Strength</td>
<td>Drives 600uA at $V_{out} = 3.5V$, and sinks 600uA at $V_{out} = 1.5V$</td>
<td>Drives 600uA at $V_{out} = 3.5V$, and sinks 560uA at $V_{out} = 1.5V$</td>
<td>Drives 150uA at $V_{out} = 3.5V$, and sinks 250uA at $V_{out} = 1.5V$</td>
</tr>
</tbody>
</table>
Testing bidirectional signals

In the absence of bidirectional control signal, testing of bidirectional signals can be performed in two ways:

- Synchronizing the directions of the bidirectional signal lines in the core and the wrapper, through proper test planning and design.
  - Disadvantage: Synchronization puts additional responsibility and overhead on the test planner and programmer.

- Place the driver in the wrapper which faces the core to be a weak driver.
  - Disadvantage: Weak driver issues like power consumption.
Weak Drivers

- Required in the absence of bidirectional control signal and difficulty of synchronization between core and wrapper.
- Can be constructed using Transmission Gates
- Operation is similar to the Buffered Memory Cell.
Strong vs weak Drivers

Characteristics of interaction of a strong driver driving logic ‘0’ and a weak driver driving logic ‘1’
Strong vs weak Drivers

Characteristics of interaction of a strong driver driving logic ‘1’ and a weak driver driving logic ‘0’

Q point for Strong driver driving logic ‘1’ and Weak driver driving logic ‘0’
Examined problems related to testing of bidirectional lines for IEEE P1500 standard.

Designed and modified bidirectional BSC structure.

Compared modified bidirectional BSC structure with the conventional structure.

- Modified bidirectional boundary scan structure utilizes 35 to 40% less transistors depending on the bus width.
- Modified structure has nearly similar propagation delays.
Summary

- Analyzed problems associated with transmission gates which were used in the modified structure and suggested solutions to it.
- Studied different signal boosting circuits to alleviate problems of driving capability and loading associated with transmission gates.
- The main signal boosting circuits studied were bus hold circuit, bidirectional repeater circuit and buffered memory cell structure.
Implementation details of conventional and the modified bidirectional boundary scan structures and also their functioning for different test instructions as prescribed by IEEE P1500 standard were discussed.

The proposed modified bidirectional boundary scan structure can be implemented successfully in designs with efficient utilization of chip area.

Structure suffers from some longer propagation delay issues which can be alleviated by use of a faster technology, efficient logic synthesis, manipulation of control signals for the control structure.

Heavy reliance on transmission gates is a shortcoming of the modified structure since not all technologies support it.
THANK YOU!

Questions?

Thank you for attending this seminar