Cypress Programmable System-on-Chip (PSoC)
Typical SoC Implementations

- Standard microcontroller
  - Limited configurability of on-chip hardware
- Custom IC
  - Build around hard or soft cores
- FPGA with “soft” cores
  - Synthesize CPUs and support functions to target gate array
- FPGA with embedded processors
  - Synthesize support functions to gate array
Peripheral functions are “fixed”, with programmable features
Custom PSoC

Functions often synthesized from IP “cores”
FPGA SoC implementation with “soft macros” (Xilinx “Picoblaze” uController)
SoC implementation using Xilinx Virtex 4 FPGA with embedded PowerPC

Configuration Memory
Control Logic
Logic Fabric
DSP Fabric
SelectIO
PowerPC™

Block Memory
Clocking & Clock Mgmt
Multi-Gigabit Transceiver

Virtex-4 Silicon Floorplan
Cypress “Programmable System on Chip” (PSoC)

- Mixed-Signal Array with On-Chip Controller
  - M8C 8-bit CPU
  - Flash, RAM & ROM memories (programs, data)
  - Configurable I/O pins
  - Programmable interconnects to on-chip modules
  - Some fixed functions (MACs, I2C, USB/WUSB)
  - Configurable blocks of digital circuits
  - Configurable blocks of analog circuits

- Lies between fixed-function microcontroller and ASIC/FPGA solutions
PSOC top-level block diagram

- Programmable I/O pins
- SRAM
- M8C CPU
- Programmable digital blocks
- ROM & Flash
- Global digital/analog interconnects
- Programmable analog blocks
- Fixed functions
# PSoC devices

## PSoC Device Characteristics

<table>
<thead>
<tr>
<th>PSoC Device Group</th>
<th>Digital I/O (max)</th>
<th>Digital Revs</th>
<th>Analog Blocks</th>
<th>Analog Inputs</th>
<th>Analog Outputs</th>
<th>Analog Columns</th>
<th>Amount of SRAM</th>
<th>Amount of Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C29x66</td>
<td>64</td>
<td>4</td>
<td>16</td>
<td>12</td>
<td>4</td>
<td>4</td>
<td>12</td>
<td>2 KB</td>
</tr>
<tr>
<td>CY8C27x43</td>
<td>44</td>
<td>2</td>
<td>8</td>
<td>12</td>
<td>4</td>
<td>4</td>
<td>12</td>
<td>256 Bytes</td>
</tr>
<tr>
<td>CY8C24x94</td>
<td>50</td>
<td>1</td>
<td>4</td>
<td>48</td>
<td>2</td>
<td>2</td>
<td>6</td>
<td>1 KB</td>
</tr>
<tr>
<td>CY8C24x23</td>
<td>24</td>
<td>1</td>
<td>4</td>
<td>12</td>
<td>2</td>
<td>2</td>
<td>6</td>
<td>256 Bytes</td>
</tr>
<tr>
<td>CY8C24x23A</td>
<td>24</td>
<td>1</td>
<td>4</td>
<td>12</td>
<td>2</td>
<td>2</td>
<td>6</td>
<td>256 Bytes</td>
</tr>
<tr>
<td>CY8C22x13</td>
<td>16</td>
<td>1</td>
<td>4</td>
<td>8</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>256 Bytes</td>
</tr>
<tr>
<td>CY8C21x34</td>
<td>28</td>
<td>1</td>
<td>4</td>
<td>28</td>
<td>0</td>
<td>2</td>
<td>4*</td>
<td>512 Bytes</td>
</tr>
<tr>
<td>CY8C21x23</td>
<td>16</td>
<td>1</td>
<td>4</td>
<td>8</td>
<td>0</td>
<td>2</td>
<td>4*</td>
<td>256 Bytes</td>
</tr>
<tr>
<td>CY7C64215</td>
<td>50</td>
<td>1</td>
<td>4</td>
<td>48</td>
<td>2</td>
<td>2</td>
<td>6</td>
<td>1 KB</td>
</tr>
<tr>
<td>CY7C603xx</td>
<td>28</td>
<td>1</td>
<td>4</td>
<td>28</td>
<td>0</td>
<td>2</td>
<td>4*</td>
<td>512 Bytes</td>
</tr>
<tr>
<td>CYWUSB6953</td>
<td>28</td>
<td>1</td>
<td>4</td>
<td>28</td>
<td>0</td>
<td>2</td>
<td>4*</td>
<td>512 Bytes</td>
</tr>
</tbody>
</table>

* Limited analog functionality.

## Availability of System Resources for PSoC Devices

<table>
<thead>
<tr>
<th>PSoC Part Number</th>
<th>USB</th>
<th>Switch</th>
<th>Mode Pump</th>
<th>Digital Clocks</th>
<th>I2C</th>
<th>Internal Voltage Reference</th>
<th>POR and LVD</th>
<th>System Resets</th>
<th>Decimator*</th>
<th>Multiply</th>
<th>Accumulate</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C29x66</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>T2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>CY8C27x43</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>T1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CY8C24x94 **</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>T2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>CY8C24x23</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>T1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CY8C24x23A</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>T1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CY8C22x13</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>T1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>CY8C21x34 **</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>CY8C21x23</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>CY7C64215 **</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>T2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>CY7C603xx **</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>CYWUSB6953</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

* Decimator types: T1 = Type 1, T2 = Type 2.
** The only PSoC devices that have the IO Analog Multiplexer system resource or USB system resource.

CYWUSB6953 = CY821x34 PSoC + WUSB6935 Radio
Supervisory ROM (SROM)

- Code for booting, flash programming, calibration

Table 3-1. List of SROM Functions

<table>
<thead>
<tr>
<th>Function Code</th>
<th>Function Name</th>
<th>Stack Space Needed</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>SWBootReset</td>
<td>0</td>
<td>72</td>
</tr>
<tr>
<td>01h</td>
<td>ReadBlock</td>
<td>7</td>
<td>73</td>
</tr>
<tr>
<td>02h</td>
<td>WriteBlock</td>
<td>10</td>
<td>74</td>
</tr>
<tr>
<td>03h</td>
<td>EraseBlock</td>
<td>9</td>
<td>74</td>
</tr>
<tr>
<td>06h</td>
<td>TableRead</td>
<td>3</td>
<td>75</td>
</tr>
<tr>
<td>07h</td>
<td>CheckSum</td>
<td>3</td>
<td>75</td>
</tr>
<tr>
<td>08h</td>
<td>Calibrate0</td>
<td>4</td>
<td>76</td>
</tr>
<tr>
<td>09h</td>
<td>Calibrate1</td>
<td>3</td>
<td>76</td>
</tr>
</tbody>
</table>
PSoC static RAM

- RAM organized in pages of 256 bytes
  - CPU has 8 address bits
  - Page register provides upper address bits

Table 4-1. PSoC Device SRAM Availability

<table>
<thead>
<tr>
<th>PSoC Device</th>
<th>Amount of SRAM</th>
<th>Number of Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C29x66</td>
<td>2 KB</td>
<td>8 Pages</td>
</tr>
<tr>
<td>CY8C27x43</td>
<td>256 Bytes</td>
<td>1 Page</td>
</tr>
<tr>
<td>CY8C24x94</td>
<td>1 KB</td>
<td>4 Pages</td>
</tr>
<tr>
<td>CY8C24x23</td>
<td>256 Bytes</td>
<td>1 Page</td>
</tr>
<tr>
<td>CY8C24x23A</td>
<td>256 Bytes</td>
<td>1 Page</td>
</tr>
<tr>
<td>CY8C22x13</td>
<td>256 Bytes</td>
<td>1 Page</td>
</tr>
<tr>
<td>CY8C21x34</td>
<td>512 Bytes</td>
<td>2 Pages</td>
</tr>
<tr>
<td>CY8C21x23</td>
<td>256 Bytes</td>
<td>1 Page</td>
</tr>
<tr>
<td>CY7C64215</td>
<td>1 KB</td>
<td>4 Pages</td>
</tr>
<tr>
<td>CY7C603xx</td>
<td>512 Bytes</td>
<td>2 Pages</td>
</tr>
<tr>
<td>CYWUSB6953</td>
<td>512 Bytes</td>
<td>2 Pages</td>
</tr>
</tbody>
</table>
General-purpose I/O pins

Eight programmable drive modes (each pin)
PSoC Digital System

Device pins
System bus (4 x 8-bit buses)
Digital blocks
1-to-4 rows of digital blocks, 4 blocks/row
Digital interconnect

VLSI Design & Test Seminar 3/21/2007
Digital block architecture

Configure for 5 functions:
- Timer
- Counter
- PWM generator
- Cyclic redundancy check
- Pseudo-random seq. gen.

Digital communications blocks:
- Master/slave SPI
- Full-duplex UART

Chain blocks for function width > 8.
Digital block data & control registers

<table>
<thead>
<tr>
<th>Function Type</th>
<th>DR0 Function</th>
<th>DR0 Access</th>
<th>DR1 Function</th>
<th>DR1 Access</th>
<th>DR2 Function</th>
<th>DR2 Access</th>
<th>CR0 Function</th>
<th>CR0 Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>Down Counter</td>
<td>R*</td>
<td>Period</td>
<td>W</td>
<td>Capture/Compare</td>
<td>RW</td>
<td>Control</td>
<td>RW</td>
</tr>
<tr>
<td>Counter</td>
<td>Down Counter</td>
<td>R*</td>
<td>Period</td>
<td>W</td>
<td>Compare</td>
<td>RW</td>
<td>Control</td>
<td>RW</td>
</tr>
<tr>
<td>Dead Band</td>
<td>Down Counter</td>
<td>R*</td>
<td>Period</td>
<td>W</td>
<td>N/A</td>
<td>N/A</td>
<td>Control</td>
<td>RW</td>
</tr>
<tr>
<td>CRCPRS</td>
<td>LFSR</td>
<td>R*</td>
<td>Polynomial</td>
<td>W</td>
<td>Seed</td>
<td>RW</td>
<td>Control</td>
<td>RW</td>
</tr>
<tr>
<td>SPIM</td>
<td>Shifter</td>
<td>N/A</td>
<td>TX Buffer</td>
<td>W</td>
<td>RX Buffer</td>
<td>R</td>
<td>Control/Status</td>
<td>RW**</td>
</tr>
<tr>
<td>SPIS</td>
<td>Shifter</td>
<td>N/A</td>
<td>TX Buffer</td>
<td>W</td>
<td>RX Buffer</td>
<td>R</td>
<td>Control/Status</td>
<td>RW**</td>
</tr>
<tr>
<td>TXUART</td>
<td>Shifter</td>
<td>N/A</td>
<td>TX Buffer</td>
<td>W</td>
<td>N/A</td>
<td>N/A</td>
<td>Control/Status</td>
<td>RW**</td>
</tr>
<tr>
<td>RXUART</td>
<td>Shifter</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>RX Buffer</td>
<td>R</td>
<td>Control/Status</td>
<td>RW**</td>
</tr>
</tbody>
</table>

7 function types
Timer & counter functions

- Data registers:
  - DR0 = synchronous down-counter
  - DR1 = period register
  - DR2 = capture/compare register

- Basic timer:
  - Count down until terminal count; reset & repeat

- Input capture:
  - capture time of an event on an input pin (DR0->DR2)

- Output compare:
  - trigger an event at a designated time (DR0=DR2)

- Counter function
  - similar to timer, except input = “gate” from an input pin
Pseudo-Random Sequence (PRS) / Cyclic Redundancy Check (CRC)

- **Registers:**
  - DR0 = linear feedback shift register (LFSR)
  - DR1 = polynomial for PRS/CRC
  - DR2 = seed value for LFSR
Serial peripheral interface (SPI) function

Data is output by both the Master and Slave, on one edge of the clock.

Data is registered at the input of both devices, on the opposite edge of the clock.

DR0 = shifter
DR1 = TX buffer
DR2 = RX buffer
UART function

- Transmitter
  - DR0 = shifter, DR1 = TX buffer
- Receiver
  - DR0 = shifter, DR2 = RX buffer
- 10 or 11-bit frame (start + 8 data + parity + stop bits)
Global Digital Interconnect
(48-pin pkg)

Input buses: GIE/GIO (pin to core logic)
Output buses: GOE, GOO (core logic to pin)

Even buses connect to pins in P0, P2, P4
Odd buses connect to pins in P1, P3, P5

One-to-many mapping. GIO[1] -> P1[1], P3[1], P5[1], etc.
Digital block row structure

"Previous" inputs always come from the previous block. Therefore, block '0' inputs come from the previous row, while block '1' inputs come from block 0, etc. If there is no previous block (i.e., there is no row above the current row), previous inputs are tied low. The chaining inputs FPB and FNB are also tied low when there is no previous block or next block.
Digital block row grouping (4 blocks/row)
Array digital interconnect

Interconnects rows of digital blocks

1 to 4 rows, depending on PSoC device.

Not configurable.
PSoC Programmable Analog Functions

- A/D converters, D/A converters
  - Delta-sigma, successive-approximation, incremental
- Amplifiers
- Comparators
- Sample & hold
- Filters
- Amplitude modulation/demodulation, FSK modulator
- Sine-wave generators, DTMF generator
- Audio drive
- Embedded modem
PSoC Analog System

- Continuous-time (CT) blocks
- Switched-capacitor (SC) blocks
- Global analog interconnect
- Reference voltages
- Input mux

Note: The CY8C21x34/23 has limited 2 column functionality.
Analog interface system

One Analog Column

Continuous Time Block
- CMP
- Latch (Transparent, PHI1 or PHI2)
- CBUS Driver

Switched Capacitor Block
- CMP (PHI1 or PHI2)
- Latch
- CBUS Driver

Switched Capacitor Block
- CMP
- Latch (PHI1 or PHI2)
- CBUS Driver

Analog Comparator Bus Slice
- Incremental Gate, One per Column (From Digital Blocks)
- Data Output
- From DBB01
- From DCB02
- From DBB11
- From DCB12

One per column
16 possible functions
For ADC

VLSI Design & Test Seminar 3/21/2007
Analog inputs to SC/CT blocks

From I/O pins
Analog reference voltages

- 3 internally-fixed reference voltages: RefHi, RefLo, AGND (programmable levels)
  - Use for ADC, DAC, Comparators, etc.
Continuous Time (CT) PSoC Block

Programmable gain/attenuation op amp circuits

Instrument amps (with 2 blocks)

Comparators

Comparator

To analog bus

Local output

Comparator bus

Low-noise/low-offset op amp

Local output

Programmable resistor string

VLSI Design & Test Seminar 3/21/2007
Example: instrumentation amp
(2 CT blocks)
Example: instrumentation amp
(2 CT blocks, one SC block)
Switched-Capacitor Blocks

- 3 arrays of binary-weighted switched capacitors
  - control movement of charge

- Applications:
  - Successive-approximation A/D
  - Sigma-delta A/D
  - Incremental A/D
  - Capacitor D/A
  - Filters

Switch settings programmed in registers
Analog switched-capacitor block (type C)

Feedback path cap array

Local output

To other analog blocks

Comparator bus

User-selectable cap arrays.
PSoC System Resources

Note: The CY8C21x34 is the only PSoC with IO Analog Multiplexer functionality.
Multiply-Accumulate (MAC)
I²C (Inter-IC) Bus Block

- 2-wire communication link
  - Serial data (SDA), serial clock (SCK)
- Supports simple networking
- Multiple-master with fixed-priority arbitration
- Speeds of 100kbps, 400Kbps, 3.4 MBps

Figure 28-1. Basic I²C Data Transfer with 7-Bit Address Format
PSoC Designer – Device Editor (select blocks)
PSoc Designer - Interconnect View