

Analyzing Reconvergent Fanouts In Min-Max Delay Fault Simulation

Hillary Grimes, Vishwani D. Agrawal

Department of ECE
Auburn University

Soumitra Bose

Intel Corporation

VLSI Design & Test Seminar – March 14, 2007

Outline

- **Introduction**
- **Problem and Approach**
- **Bounded Gate Delay Fault Simulation**
- **Reconvergent Fanout Analysis**
- **Hazard Simulation Algorithm**
- **Results**
- **Future Work**

Introduction

- **Roboust Tests**
 - Independent of circuit delays
 - Highest quality, but few faults are robustly testable
- **Nonroboust Tests**
 - Easily invalidated by hazards due to off path gate delays
 - Test quality determined by both detection of delay faults, and sizes of detectable delay faults

Introduction

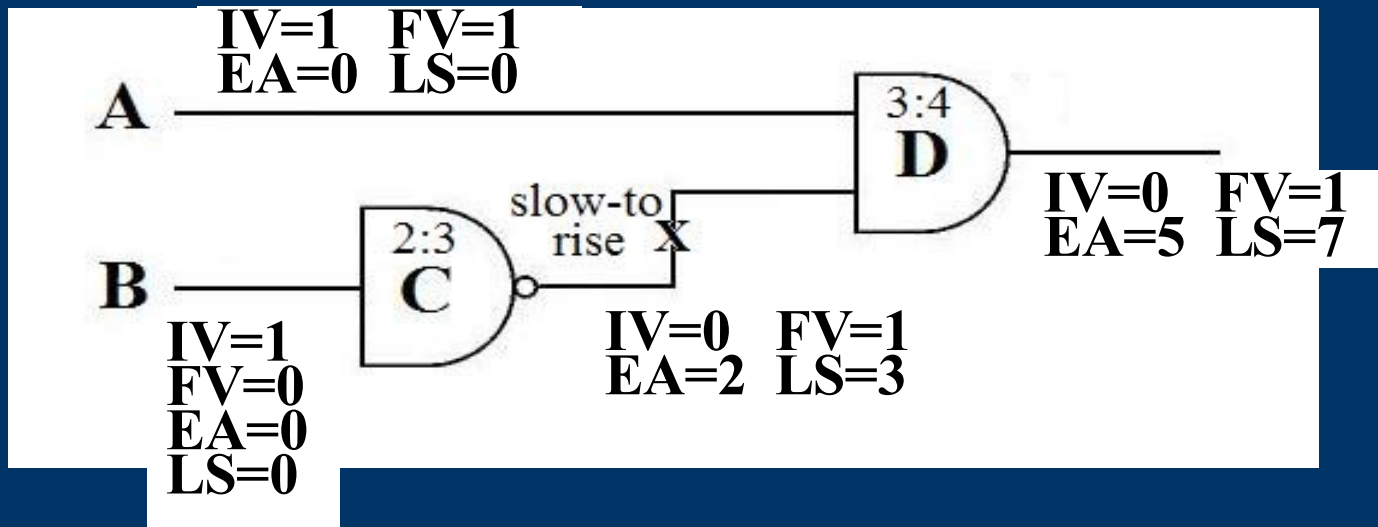
- **Transition Fault Model**
 - Gate oriented model
 - Faults delay rising and falling transitions
 - Two types: slow-to-rise and slow-to-fall
 - To test a slow-to-rise transition fault, V1 puts a 0 at the fault site, and vector V2 is a test for the stuck-at-0 fault at the fault site
- **Bounded Delay Fault Simulation**
 - Allows for imprecise gate delays
 - Gate delays specified as a range
 - D – Max Delay
 - d – Min Delay

Problem & Approach

- **Problem**
 - Bounded delay fault simulation lacks reconvergent fanout analysis
 - This results in pessimistic calculation of detectable delay fault sizes
- **Approach**
 - Propagate *Hazard Lists*, which contain fanout information.
 - Consider fanout information when evaluating reconvergent gates

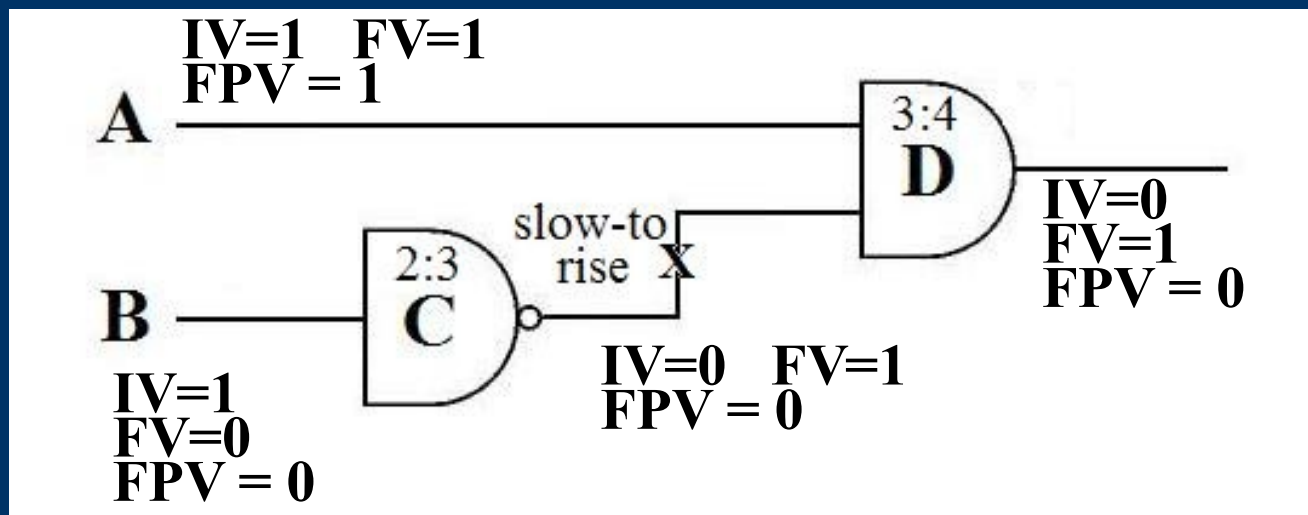
Bounded Gate Delay Fault Simulation

- Faultless Circuit Calculations
 - IV: Initial Logic Value
 - FV: Final Logic Value
 - EA: Earliest Arrival Time
 - LS: Latest Stabilization Time



Bounded Gate Delay Fault Simulation

- Faulty Circuit Calculations
 - δ : Fault Size
 - FPV: Fault Propagating Value
 - At Fault Site - $FPV = IV$
 - Outside downcone of fault site - $FPV = FV$
 - Inside downcone of fault site
 - $FPV = \text{Logic Value at that gate with a stuck fault at the fault site}$



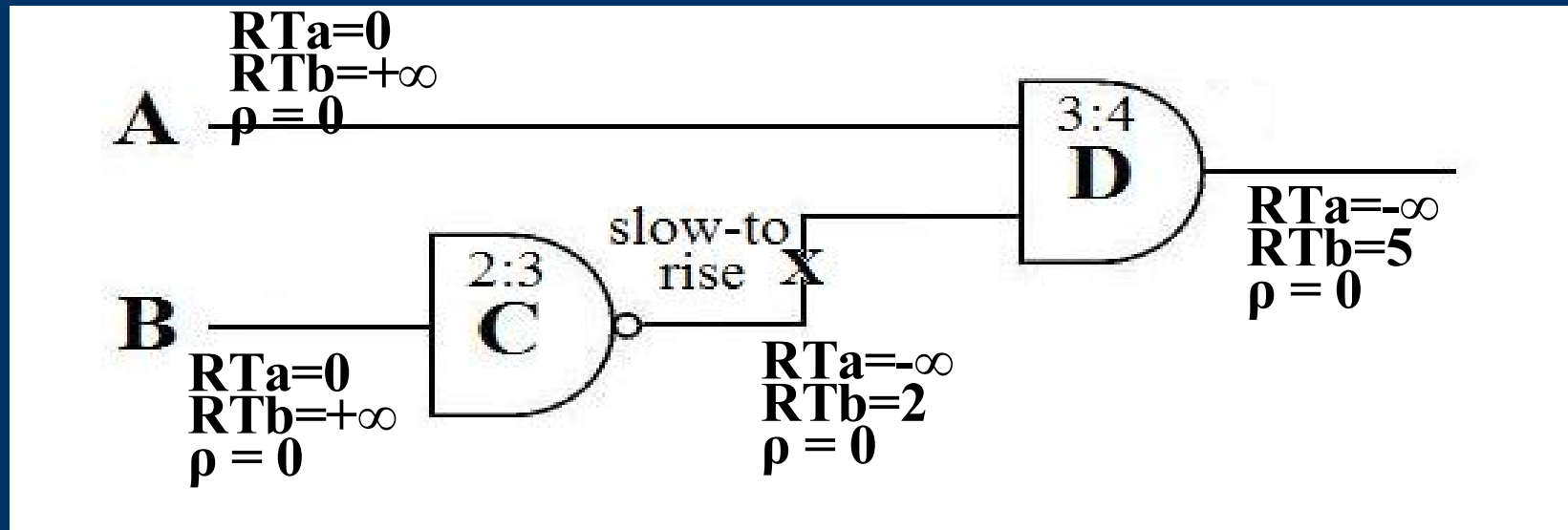
Bounded Gate Delay Fault Simulation

- Reference Quantities
 - ρ : Reference Fault Size
 - RTa & RTb : Reference Times
 - Waveform is at FPV inside the interval of time from RTa to $RTb + \delta$, provided that $\delta > \rho$
- At fault site
 - $\rho = 0$
 - $RTa = -\infty$
 - $RTb = EA(\text{ fault site })$
- Outside downcone of fault site
 - $\rho = 0$
 - $RTa = LS(\text{ fault site })$
 - $RTb = +\infty$

Bounded Gate Delay Fault Simulation

- Inside Downcone of Fault Site
- Case 1
 - No inputs (i) have a dominate FPV value
 - $w = \max(0, \max(RTa(i)) + D - \min(RTb(i)))$
 - $\rho = \max(\max(\rho(i)), w)$
 - $RTa = \max(RTa(i)) + D$
 - $RTb = \min(RTb(i)) + d$
- Case 2
 - Some input FPVs are dominant
 - Choose dominant FPV input with minimum ρ
 - $\rho = \max(\rho(i), RTa(i) + D - RTb(i))$
 - $RTa = RTa(i) + D$
 - $RTb = RTb(i) + d$

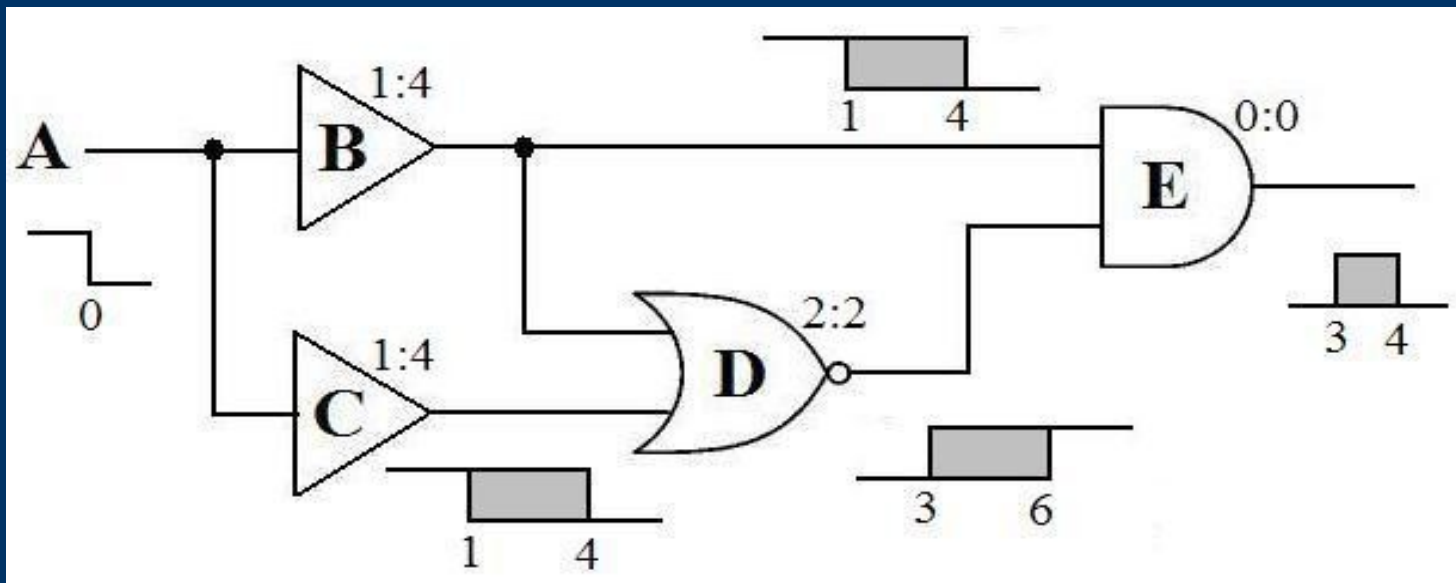
Bounded Gate Delay Fault Simulation



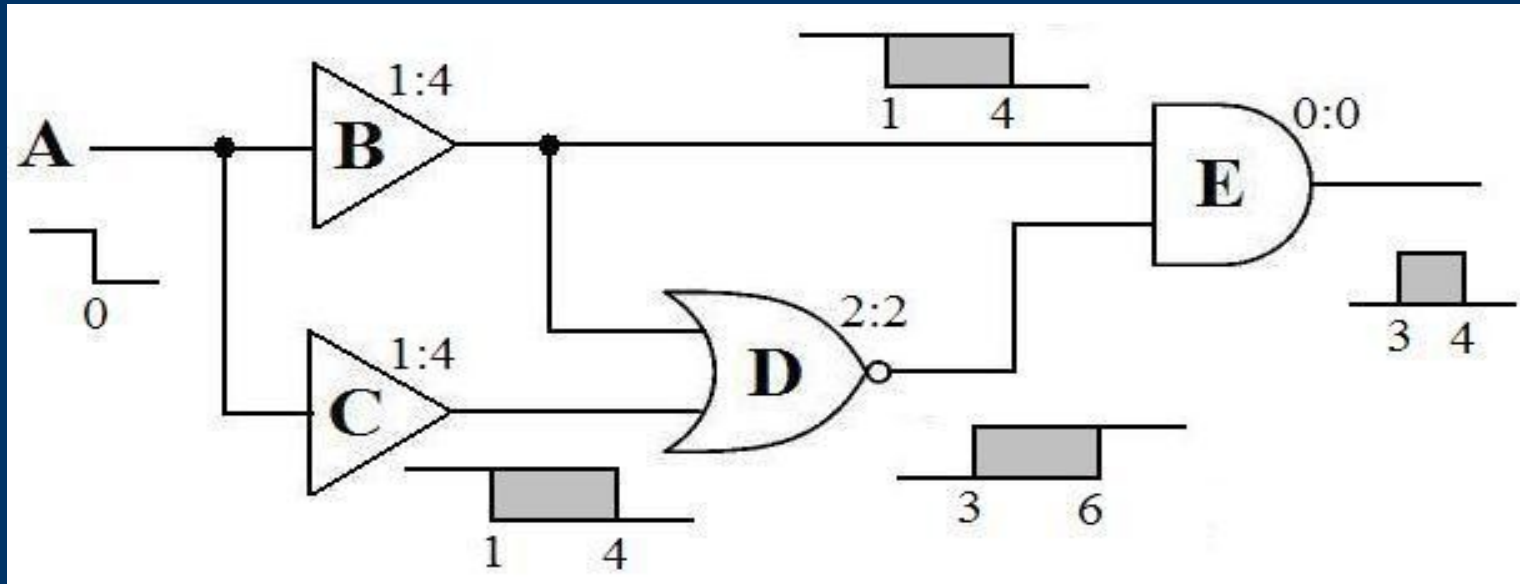
- **Detection Threshold**
 - $\max(\rho(D), \text{Obs}(D) - RTb(D))$
- **Suppose we sampled the output at time 7**
 - Threshold = $7 - 5 = 2$
 - Minimum size gate delay fault guaranteed to be detected is 2

Analyzing Reconvergent Fanouts

- Certain time correlations at the inputs of reconvergent gates can guarantee no hazard will occur at the output
- For example, consider the hazard produced at gate E:

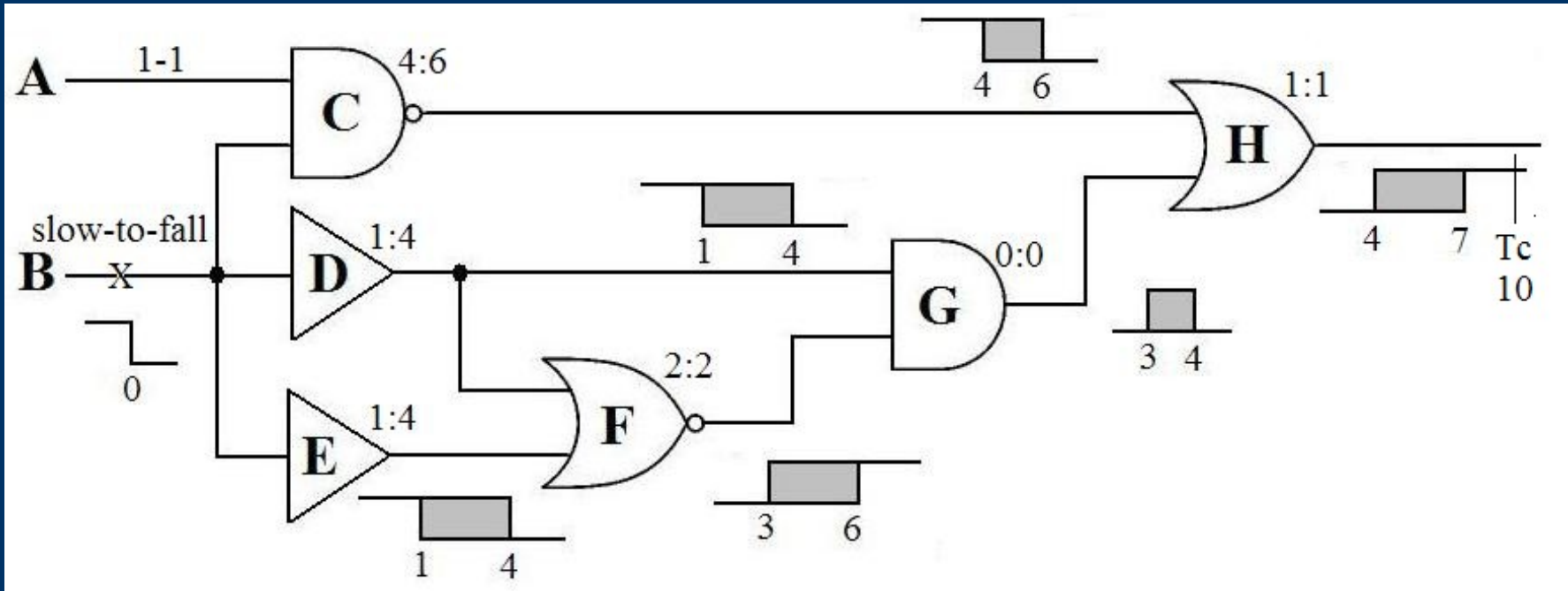


Analyzing Reconvergent Fanouts



- Static hazard produced at the output from 3 to 4 time units never occurs in an actual circuit
- Time-correlations at the inputs of gate **E** guarantee the rising edge on **D** never precedes the falling edge on **B**

Analyzing Reconvergent Fanouts



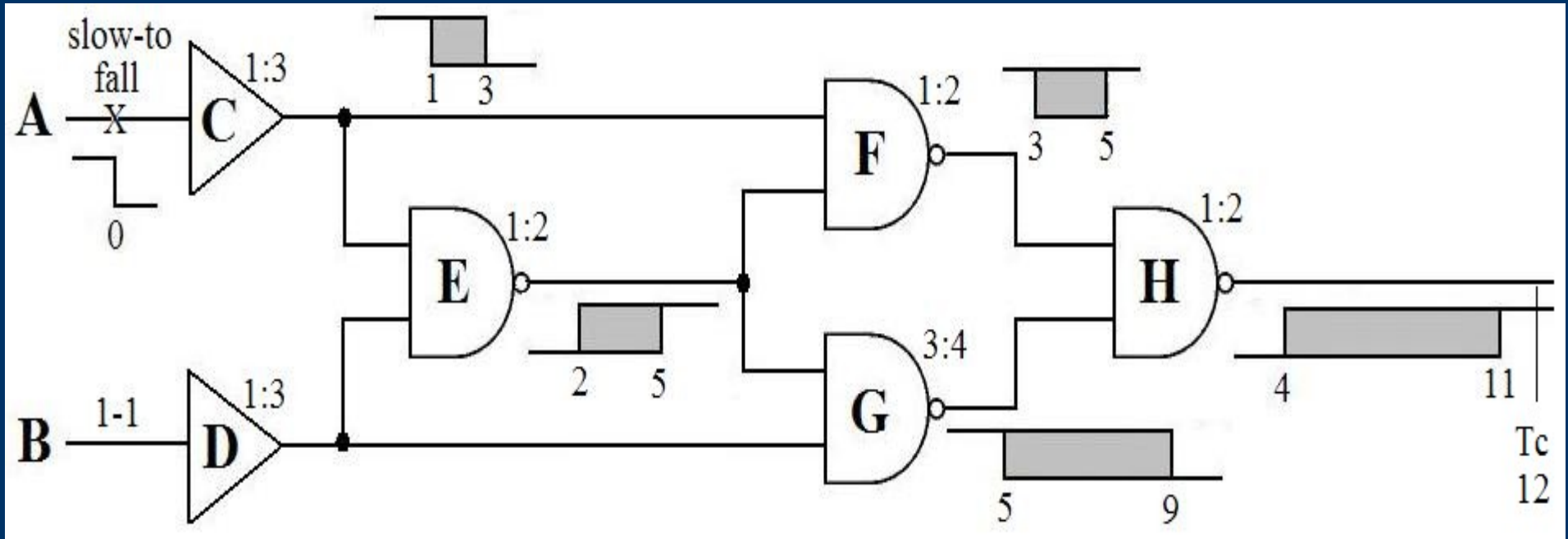
- Static hazard on gate G is erroneous, similar to the previous example

Analyzing Reconvergent Fanouts

Signal	EA	LS	FPV	ρ	RTa	RTb
A	∞	$-\infty$	1	0	$-\infty$	∞
B	0	0	1	0	$-\infty$	0
C	4	6	0	0	$-\infty$	4
D	1	4	1	0	$-\infty$	1
E	1	4	1	0	$-\infty$	1
F	3	6	0	0	$-\infty$	3
G	3	4	0	0	$-\infty$	3
H	4	7	0	0	$-\infty$	4

- Suppose we sampled the output at time 10
 - Threshold = $10-4 = 6$
- Minimum size gate delay fault guaranteed detected is 6, but should be 5

Analyzing Reconvergent Fanouts



- Static hazard on gate F is erroneous, similar to the previous example

Analyzing Reconvergent Fanouts

Signal	EA	LS	FPV	ρ	RTa	RTb
A	0	0	1	0	$-\infty$	0
B	∞	$-\infty$	1	0	$-\infty$	∞
C	1	3	1	0	$-\infty$	1
D	∞	$-\infty$	1	0	$-\infty$	∞
E	2	5	0	0	$-\infty$	2
F	3	5	1	0	$-\infty$	3
G	5	9	1	0	$-\infty$	5
H	4	11	0	0	$-\infty$	4

- Suppose we sampled the output at time 12
 - Threshold = $12 - 4 = 8$
- Minimum size gate delay fault guaranteed detected is 8, but should be 6

Hazard Simulation Algorithm

- **Each gate G has a hazard list**
 - Gate ids of fanout points that lie in the forward cone of the delay fault site
 - Minimum delay from fanout point to G
 - Maximum delay from fanout point to G
- **Hazard list propagation is similar to fault list propagation in concurrent fault simulation**

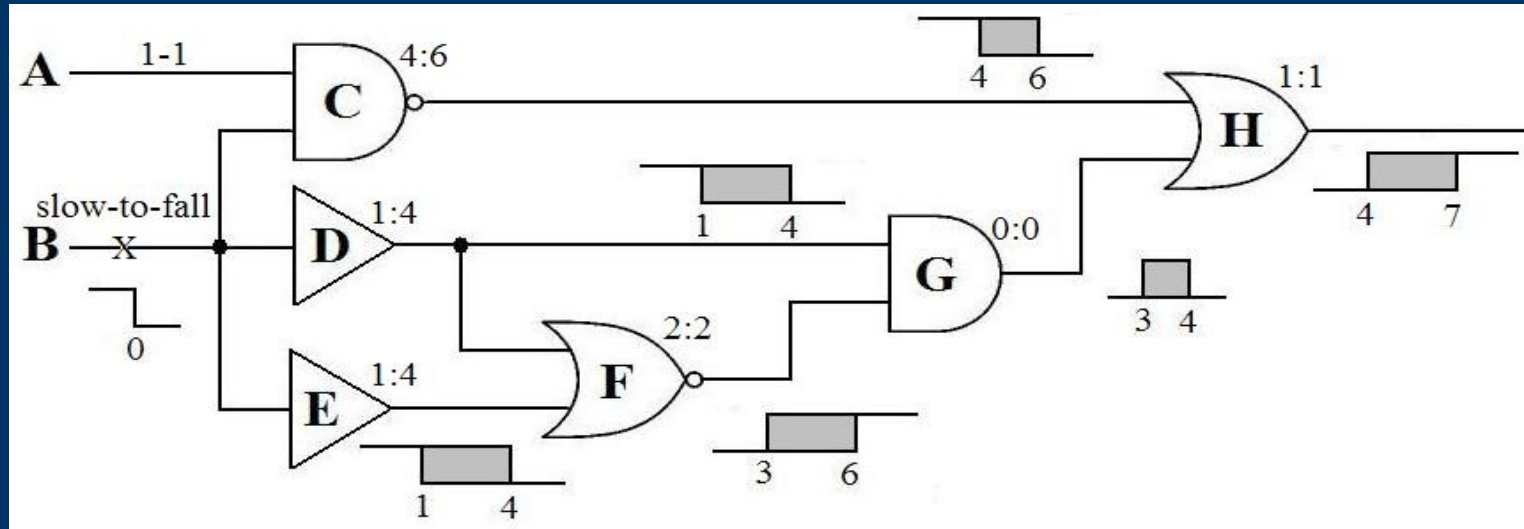
Hazard Simulation Algorithm

- **Hazard Lists are evaluated for each gate in the downcone of the fault site**
- **Case 1**
 - **No inputs (i) have a dominate FPV value**
 - **For every entry in the hazard lists of inputs, a new entry is added to hazard list at G containing**
 - **Id of fanout point**
 - **Minimum delay from fanout point to G**
 - **Maximum delay from fanout point to G**

Hazard Simulation Algorithm

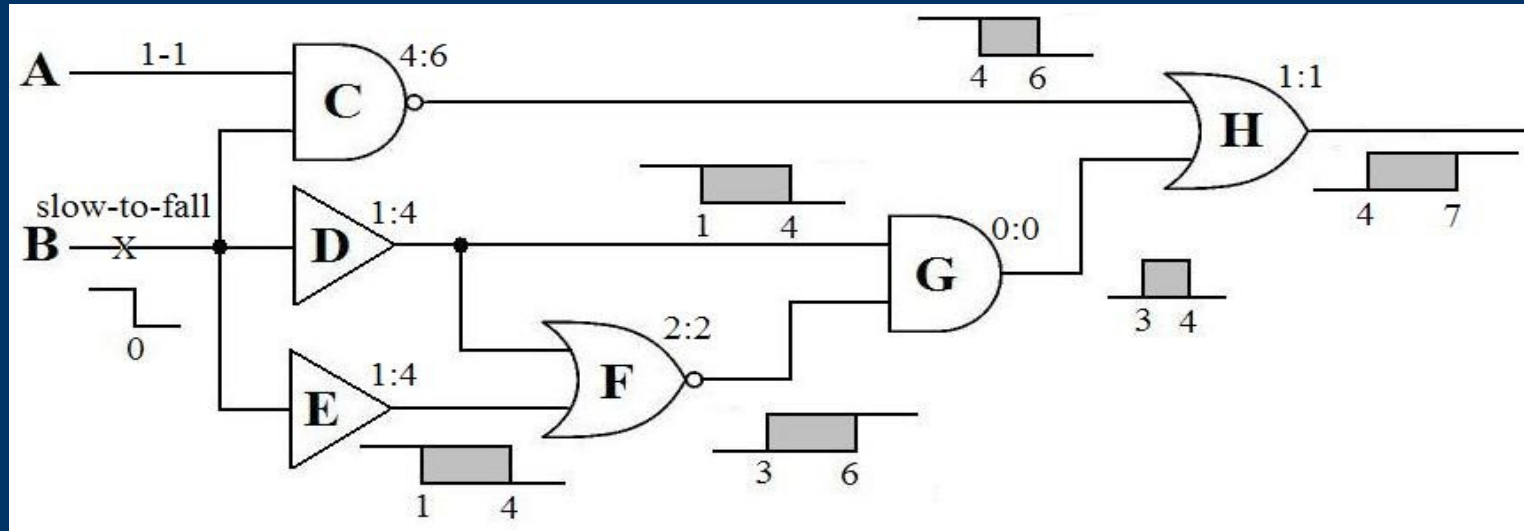
- **Case 2**
 - Some input FPVs are dominant
 - For all fanout points that appear in hazard lists of all inputs
 - $\text{mindv} = \max(\text{min delay from fanout point to input with dominant FPV})$
 - $\text{maxsv} = \max(\text{max delays from fanout point to input with non-dominant FPV})$
- **If $\text{mindv} > \text{maxsv}$**
 - Hazard is suppressed
 - $\rho = 0$
 - $\text{RTa} = -\infty$
 - $\text{RTb} = \infty$
 - Hazard list for G is set to NULL

Hazard Simulation Algorithm List Propagation



C D E Propagating Hazard list to output of F
 B(4,6) $\left. \begin{matrix} B(1,4) \\ D(0,0) \end{matrix} \right\}$ B(1,4) produces: $\left. \begin{matrix} B(3,6) \\ D(2,2) \end{matrix} \right\}$

Hazard Simulation Algorithm List Propagation

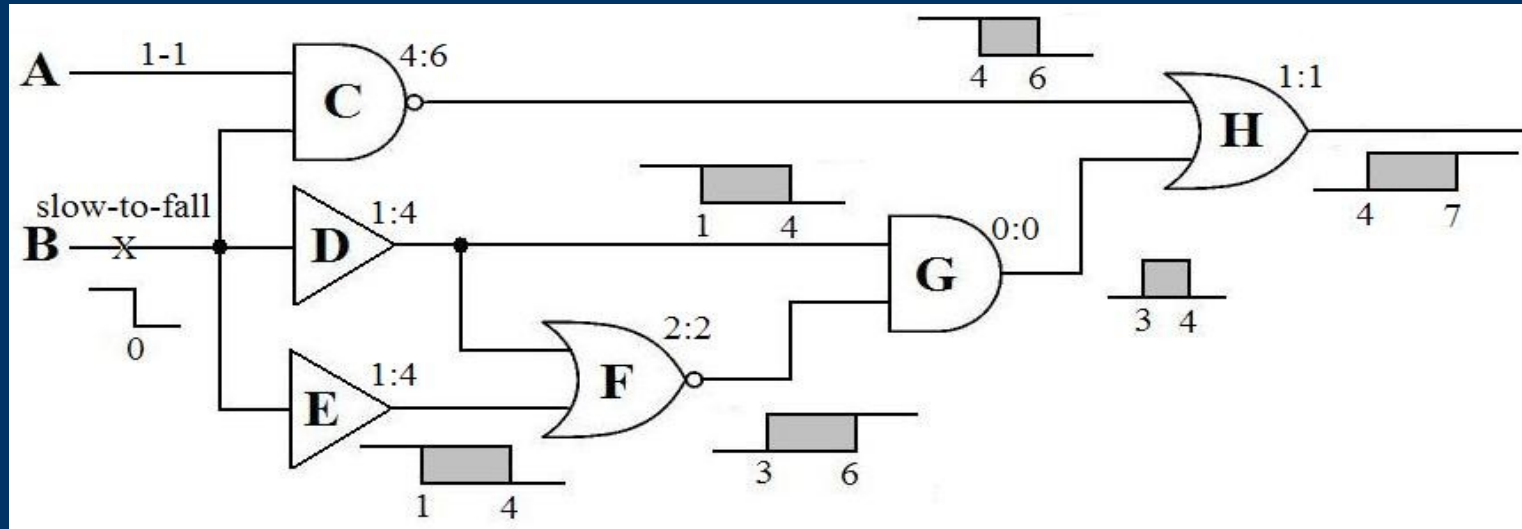


C	D	E	F
B(4,6)	B(1,4) D(0,0)	B(1,4)	B(3,6) D(2,2)

Propagating Hazard list to output
of G:
mindv=2
maxsv=0

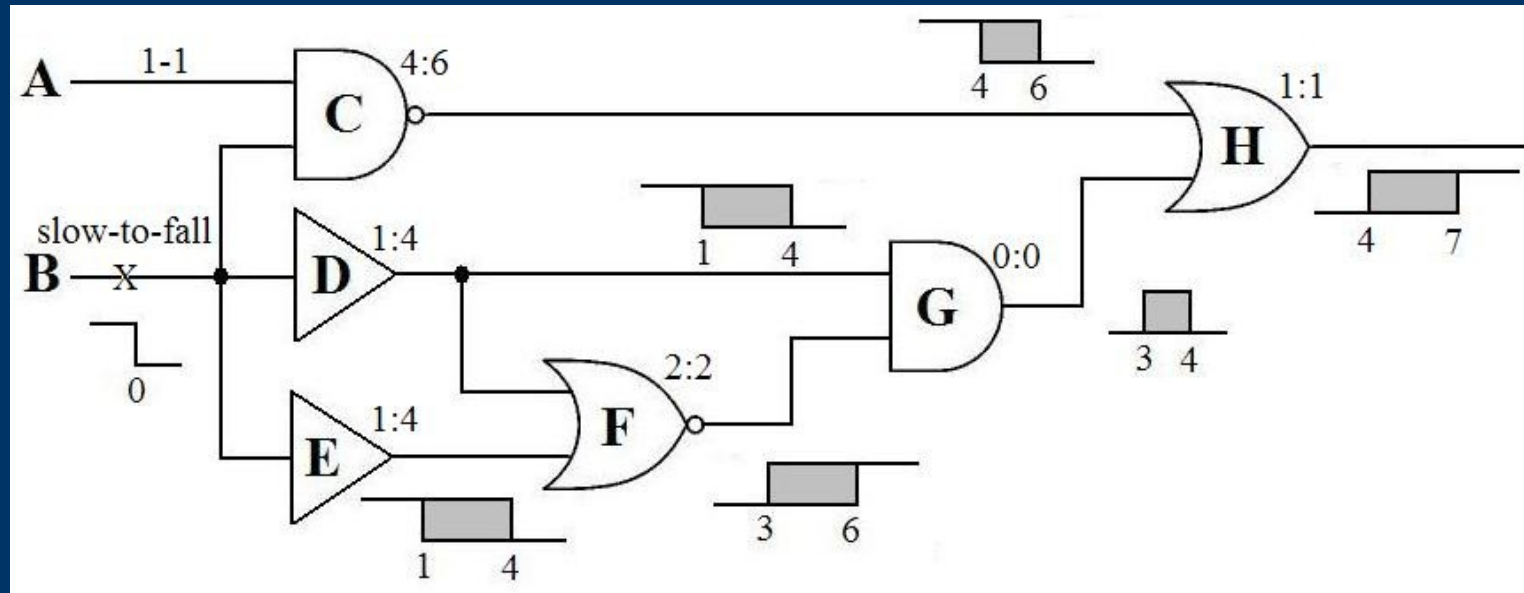
Mindv > Maxsv
Hazard Suppressed & hazard
List at G=Null

Hazard Simulation Algorithm List Propagation



C D E F Propagating Hazard list to output
 of H: B(5,7)
 B(4,6) B(1,4) B(1,4) B(3,6)
 D(0,0) D(2,2)

Hazard Simulation Algorithm



Signal	FPV	ρ	RTa	RTb	Hazard List
A	1	0	$-\infty$	∞	Null
B	1	0	$-\infty$	0	(B,0,0)
C	0	0	$-\infty$	4	(B,4,6)
D	1	0	$-\infty$	1	(B,1,4) (H,0,0)
E	1	0	$-\infty$	1	(B,1,4)
F	0	0	$-\infty$	3	(B,3,6) (H,2,2)
G	0	0	$-\infty$	∞	Null
H	0	0	$-\infty$	5	(B,5,7)

Hazard Simulation Algorithm

Signal	FPV	ρ	RTa	RTb	Hazard List
A	1	0	$-\infty$	∞	Null
B	1	0	$-\infty$	0	(B,0,0)
C	0	0	$-\infty$	4	(B,4,6)
D	1	0	$-\infty$	1	(B,1,4) (H,0,0)
E	1	0	$-\infty$	1	(B,1,4)
F	0	0	$-\infty$	3	(B,3,6) (H,2,2)
G	0	0	$-\infty$	∞	Null
H	0	0	$-\infty$	5	(B,5,7)

- Hazard at gate G is suppressed
- Threshold evaluated correctly
 - Threshold = $10 - 5 = 5$

Results

Circuit	Gate Faults	Coverage (%)	Bounded Delay Fault Simulation	BDFS with Hazard Suppression
c432	420	97.1	42.6	42.6
c499	564	97.9	96.9	71.2
c880	952	98.7	35.6	15.6
c1355	1252	99.0	59.2	54.2
c1908	1890	98.9	35.9	26.1
c2670	3298	98.9	26.1	21.4
c3540	3496	70.7	16.7	8.1
c5315	5230	99.8	12.4	8.2
c7552	7666	99.2	12.0	9.0

- Coverage High – slow-to-transistion at gate output always detected with some threshold
- Columns 4 and 5 consider detected faults on critical paths (70% of the longest path)

Future Work

- **General analysis of reconvergent fanouts**
 - How does this analysis effect static timing analysis?
 - **Timing Simulation?**
 - **Dynamic Timing Analysis?**

Acknowledgment: We would like to thank Dr Soumitra Bose of Intel for contributions to this research, including implementation and results