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**ACHIEVEMENTS:** transmission of a block coded PCM signal over a noisy baseband channel; comparison of 7-bit linear versus 4-bit block coded PCM.

**PREREQUISITES:** completion of the experiment entitled *Block coding and decoding* in this Volume.

**ADVANCED MODULES:** PCM ENCODER, PCM DECODER (version 2 or later), BLOCK CODE ENCODER, BLOCK CODE DECODER, LINE-CODE DECODER, LINE-CODE ENCODER, NOISE GENERATOR. A WIDEBAND TRUE RMS METER is optional.

**PREPARATION**

This experiment is an extension of the introductory experiment entitled *Block coding and decoding* in this Volume.

The extension involves the transmission of the coded signal via a noisy baseband channel.

Since the message is analog, the evaluation of performance is made by measuring the recovered message signal-to-noise ratio under different conditions. This can be a quantitative measurement, using the WIDEBAND TRUE RMS METER, otherwise qualitative by observation of the recovered periodic message waveform.

You are free to determine which measurements are of interest. The Tasks outlined below are there to guide you in setting up the system.

**system parameters**

Clock speeds and message frequencies are determined by the DECISION MAKER, which has an upper rate of operation. Thus:

1. the DECISION MAKER module has a clock rate limited to the vicinity of 2 kHz, so a rate of 2.083 kbit/sec has been chosen.
2. the BLOCK CODE ENCODER operates on blocks (or frames) of eight bits. These are provided by a PCM ENCODER.

3. to provide room for coding bits within the frame, which is of 8-bit width, the PCM ENCODER will operate in the 4-bit mode.

4. for an eight bit frame the sampling rate will be 260 samples/sec (2083/8).

5. the maximum message frequency will be limited to 130 Hz (Nyquist). This is below the range of the AUDIO OSCILLATOR module. But there are four fixed-frequency sinusoidal (and near-sinusoidal) messages available within the PCM ENCODER module. Their frequencies, and access details, are given in the Appendix to this experiment.

A TUNEABLE LPF will be used for the bandlimiting channel, according to the scheme detailed in the experiment entitled The noisy channel model in volume D1.

A simplified block diagram of the system is shown in Figure 1.

![Figure 1: the system block diagram](image)

**EXPERIMENT**

The block diagram of Figure 1 can be modelled as shown in Figures 2 to 4

**transmitter**

![Figure 2: the transmitter](image)
**T1** patch up the transmitter model of Figure 2. It is convenient to use DC for the message during the setting up procedure. Select the 4-bit LINEAR PCM code, and PARITY block coding.

**channel**

![Diagram of the channel model](image)

**T2** patch up the noisy channel according to Figure 3.

**T3** disconnect any DC from the output ADDER input.

**T4** observe the wave shape at the channel output for full channel bandwidth, then tune the filter until there is obvious bandlimiting. See Tutorial Question Q1.

**T5** with full output from the noise source set the SNR at the DECISION MAKER input output to a few dB (by oscilloscope observation), and at about the TIMS ANALOG REFERENCE LEVEL.

**T6** reduce the noise by the full available attenuation of the NOISE GENERATOR front panel attenuator.

The signal is now ready for demodulation, presumably without errors, since the SNR should be well above 0 dB (above 22 dB).
T7 patch up the receiver of Figure 4 below.

![Figure 4: the receiver model](image)

T8 with the channel output connected to the DECISION MAKER input, while observing either an eye pattern or a snapshot display, and using the decision instant marker, adjust the decision instant. See Tutorial Question Q2.

T9 ensure matching line codes are selected at both transmitter and receiver. NRZ-L is suggested.

T10 at the BLOCK CODE DECODER select frame synchronization using the EMBEDded frame synch. signal, and PARITY block coding.

T11 at the PCM DECODER select 4-bit LINEAR decoding and frame synchronization using the EMBEDded frame synch. signal.

T12 check the bit clock patching. Note that the STROBE from the LINE-CODE DECODER is not used.

Now check signals and waveforms from input to output. The message is DC. The oscilloscope displays should be stable and identifiable if the FS signal is used as the oscilloscope synchronization signal.

T13 identify a frame at the output of the PCM ENCODER (CH1-A), and follow it through the BLOCK ENCODER and the LINE-CODE ENCODER to the channel input.

T14 while looking at your chosen frame entering the channel (CH1-A), locate it on the other oscilloscope trace (CH2-A) at the channel output.
T15 move CH2-A forward to the output of the DECISION MAKER and confirm the regeneration of the desired wave shape.

T16 move CH1-A back one stage to the input of the LINE-CODE ENCODER, and CH2-A forward to the LINE-CODE DECODER output. Confirm the two waveforms agree in shape, and that there is a delay. See Tutorial Question Q3.

T17 if considered necessary, fine trim the DC level to match the threshold (about +25 mV) of the DECISION MAKER.

**evaluation**

You will not be making bit error rate (BER) measurements using the BER instrumentation techniques investigated in earlier experiments. These required a precise knowledge of the signal-to-noise ratio at the decision device input, and a known data sequence for bit-by-bit comparison.

Instead you are looking for changes in SNR (or waveform quality) of the recovered output message. A measure of error rates is available from the error detector circuitry of the BLOCK CODE DECODER module. The error rate can be used as a reference condition.

The noise at the output will be made up of quantization noise (unavoidable), errors introduced by the noise added to the signal, and perhaps distortion components. See Tutorial Question Q4.

There are many ‘A - B’ comparisons which can now be made.

Most evaluations will be qualitative, by observing the recovered sinusoidal message via the built-in reconstruction filter of the PCM DECODER, under the two conditions ‘A’ and ‘B’.

The error counter in the BLOCK CODE DECODER will be used as a guide to the digital errors (caused by noise) in the ‘A’ state, but cannot be used as a comparison measure, since the ‘B’ state will generally not be using block coding.

The technique is to reduce the SNR until a change is seen in the reconstituted message waveform under condition ‘A’. Then, with this SNR, to switch to condition ‘B’ and to look for a variation in the message waveform (or, with the WIDEBAND TRUE RMS METER, to measure a change of SNR, or SNDR ¹).

It is important that the reconstruction filter does not prevent message distortion being observed. Thus it is important to ensure that:

- the reconstruction filter bandwidth is close to the Nyquist bandwidth (ie, as wide as possible)
- the message frequency is low enough to allow the passage of at least an even (2nd) and an odd (3rd) harmonic through the reconstruction filter.

Suggested comparisons could be:

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¹ signal-to-noise-plus-distortion ratio
• 4-bit PCM encoding with and without block coding
• 7-bit linear PCM encoding (no block coding) versus 4-bit linear PCM
• 7-bit linear PCM encoding (no block coding) versus 4-bit linear PCM encoding with block coding

Remember that there are three block codes to investigate for each case involving block coding.

**T18** carry out as many of the above ‘A - B’ comparisons as you consider important. Compare with expectations.

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**TUTORIAL QUESTIONS**

**Q1** it was suggested in Task T4 that you adjust the channel bandwidth until there was ‘obvious bandlimiting’. How did you decide on the bandwidth, and why?

**Q2** describe your method of adjusting the decision instant.

**Q3** what was the approximate signal delay between input and output of the system? What factors contribute to this delay? If more than one source of delay, could you attribute contributions to each source?

**Q4** some of the observations made were of output SNR. The noise here was made up of at least three components, namely quantization noise, intentionally added noise, and distortion components. How were these accounted for in your findings?

**Q5** describe observations you made, not included as specific Tasks, and your conclusions.
For a MASTER CLOCK of 8.333 kHz, Table A-1 below gives the frequencies of the synchronized message at the SYNC. MESSAGE output for the setting of the onboard switch SW2.

For other clock frequencies the message frequency can be calculated by using the ‘divide by’ entry in the Table.

These messages are periodic, but not necessarily sinusoidal in shape. The term ‘sinuous’ means sine-like.

<table>
<thead>
<tr>
<th>LH toggle</th>
<th>RH toggle</th>
<th>divide clock by</th>
<th>freq with 8.333kHz clock</th>
<th>approx. ampl. and waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td>UP</td>
<td>UP</td>
<td>32</td>
<td>260.4 Hz</td>
<td>0.2 $V_{pp}$ sine</td>
</tr>
<tr>
<td>DOWN</td>
<td>UP</td>
<td>64</td>
<td>130.2 Hz</td>
<td>2.0 $V_{pp}$ sine</td>
</tr>
<tr>
<td>UP</td>
<td>DOWN</td>
<td>128</td>
<td>65.1 Hz</td>
<td>4.0 $V_{pp}$ sinuous</td>
</tr>
<tr>
<td>DOWN</td>
<td>DOWN</td>
<td>256</td>
<td>32.6 Hz</td>
<td>4.0 $V_{pp}$ sinuous</td>
</tr>
</tbody>
</table>

Table A-1