Introduction to Digital and Analog IC Designs

Topics

• Introduction to Wireless Communications (1.5 classes)
• Basic Concepts for Integrated Circuits (3 classes)
• Analog IC Design Using Cadence Analog IC Design Tools (2.5 classes)
• Switching and Logic Circuits (1.5 classes)
• Bandgap Reference and Current Mirrors (2.5 classes)
• Exam I (1 class)
• Amplifiers (3 classes)
• Oscillators (2 classes)
• Digital IC Design Using Verilog HDL (3 classes)
• Digital Frequency Dividers (1 class)
• Digital Delta-sigma Modulators (2.5 classes)
• Exam II (1 class)
• Digital Phase Locked Loop (1 class)
• Conclusions and Final Reviews (1 class)
• Final Project Presentation (1 class)
• Final Project Report
Chapter 3
Cadence® Analog Design Environment

• Getting started with Cadence Tool
• Schematic Editor
• Project

Cadence tool information @
http://www.cadence.com/datasheets/

It supports RF/Analog and mixed-signal simulation
Required Software

• Xming: is a free software port of the X Window Server to Microsoft Windows. Xming-fonts is required to display fonts correctly.

  ![Xming-6-9-0-31-setup.exe](image1.png)
  ![Xming-fonts-7-5-0-47-setup.exe](image2.png)
  
  • Secure CRT6.75:
Access Workstations

• SecureCRT 6.75 and Xming
  – First, double click Xming to start the window interface for the workstation we will use.
  – Then, double click SecureCRT 6.75 and you will see a log-on window as shown in next slide.
Setup for SecureCRT

- Right click “Engineering” and click Properties
When you open secureCRT, go to “Session Options”, select “Remote/X11” and check “Forward X11 packets”. Then click OK.
How to login to a workstation

1. Click connect
2. Type in your username and password
3. Enter SSH Username
4. Enter Secure Shell Password

- Click connect and then type in your username and password
SecureCRT Interface

- Press “Enter”
- Then type “yes” and press “enter”
- Type your password and “enter”
How to login to a workstation

• When the system prompts “Please enter the name of an Engineering host <anywhere>:”, just enter and input password. It will randomly select a workstation for you to use. The workstation name should starting with “tux” and ending with a number.
• Type “xterm” then you will see a pop-up window.
• Copy the class-provided .bashrc file to your home directory (“~” is your home directory).
• Type “source .bashrc” when you are under home directory.
Setup Cadence Tool

• Creat your own starting directory for your cadence by using command “mkdir class”
• Copy the cadence configuration files to this newly created directory. Those files include .cdsenv .cdsinit display.drf cds.lib.
• From your “class” directory, type “icfb&” to start cadence.
Design System Initialization Files

- **.bashrc or .cshrc and .login** → configure the operating system environment and the UNIX environment when you login and start a UNIX application. (Linux environment is preferred)

- **.cdsinit** → customizes the Affirma Analog Circuit Design Environment.

- **.cdsenv** → configure Cadence Analog Artist tool environment.

- **cds.lib** → set paths to the libraries used by the Analog Artist software.
  
  **Cadence default lib:**
  
  INCLUDE /linux_apps/cadence/IC/share/cdssetup/cds.lib

  **User defined lib:**
  
  DEFINE sige5am /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/sige5am
  DEFINE Dai6970 ~/elec6190/Dai6970

- **Cadence process design kit (PDK) can be downloaded** [www.cadencePDK.com](http://www.cadencePDK.com)
Start Cadence Tool

• **icfb&**  ➔ front to back design,
  default CDS_Netlisting_Mode “Digital”

• **icms&**  ➔ mixed signal design,
  default CDS_Netlisting_Mode “Digital”

• **msfb&**  ➔ mixed signal front to back design,
  default CDS_Netlisting_Mode “Analog“, don’t need to add setenv
  CDS_Netlisting_Mode "Analog" in **.bashrc** or **.cshrc**.

• Schematic cellview to cellview defaults for creating a symbol with Artist.
  The default is to not create an Artist symbol.
  The following has been added in .cdsinit:
  
  ```
  schSetEnv("tsgTemplateType" "artist")
  ```
Initializing Design Framework II Environment

The Design Framework II software reads your .cdsinit file at startup to set up your environment.

.cdssinit:
Sets user-defined bindkeys.
Redefines system-wide defaults.
Contains SKILL commands.

The search order for the .cdsinit file is:
<Filename><install_dir>/tools/dfII/local
the current directory [Name6970] ← put .cdsenv, .cdsinit, cds.lib here
the home directory

When a .cdsinit file is found, the search stops unless a command in .cdsinit reads other files.

Path to a sample .cdsinit file:
<Filename><install_dir>/tools/dfII/samples/artist/cdsinit
<install_dir>=/opt/cadence/ic5.033
Summary of Cadence Tool Setup

1) Sign Non-Disclosure Agreement.
   During the course, students (“Receiving Party”) may receive or use information regarding analog and digital IC design tools and processing technology libraries. The receiving party agrees to keep any information received during the course strictly confidential and NOT to disclose any information regarding the class notes, EDA tools and technology libraries to any party outside of the class. Upon the completion of the class, the access to the technology files should be removed and the manuals and any other information related to the technology files should be destroyed.

2) Copy .bashrc to your home directory
3) Place .cdsenv and .cdsinit files at your launch directory.
4) Place or update cds.lib file at your launch directory. Make sure to include:
   INCLUDE /linux_apps/cadence/IC/share/cdssetup/cds.lib
   DEFINE sige5am /class/ibm_lib/5am/IBM_CDS/sige5am/reIAM/sige5am
5) Type “icfb&” to launch the tool.
6) Go though Cadence “Virtuoso® Schematic Composer Tutorial”
8) Further reading on layout: “Cell Design Tutorial” and “Virtuoso Layout Editor User Guide”
Analog Circuit Simulator Setup

- Select Tools>Analogue Environment to see the simulator.

- Setup --> Model Library:
  /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/design.scs
  /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/process.scs
- Make sure design.scs is above process.scs

- Setup --> Simulation Files:

  Include Path: /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre

  Definition Files: definitions.scs

- The above steps were saved in a state file. In class directory, under Cadence, copy the “state_template” directory to your unix directory: ~/.artist_states/your_lib/your_design/spectre/. Then, load this state in Cadence “Analogue Environment under tools”.

IBM manuals located at:
/class/ibm_lib/5am/IBM_CDS/sige5am/relAM/doc
Summary of Cadence Setup Procedure

(1). Change IC tools version to 5.141. It can be done with the user setup interface or manually.
(2). Add sige5am library. Choose /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/sige5am using library path editor, save it. The relAM is a symbol link to V2.3.0.5AM, you can use V2.3.0.5AM as well.
(3). Copy .cdsinit and .cdsenv from /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/examples/ to your working directory. You may want to use Cadence binding key instead of that from IBM, just comment out or delete the line contains Key binding in the file .cdsinit (add the write permission: chmod +w .cdsinit).
(4). Setup CDS_Netlisting_Mode variable.
   - If you use CSH, add this to the ~/.cshrc: setenv CDS_Netlisting_Mode Analog
   - If you use BASH, add this to the ~/.bashrc: export CDS_Netlisting_Mode Analog
(5). Add AMS property to your design library: select from the CIW menu, IBM_PDK ->library->Add A&MS properties. A dialog will pop up, then choose the library name as your design library name and the technology such as sige5am. The other two options are number of the metal layers and type of the capacitor, you can leave it as default.
(6). During the simulation, add model and definition files.
   - Setup --> Model Library:
     /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/design.scs
     /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/process.scs
   - Setup --> Simulation Files:
     include path: /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre
     definition files: /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/definitions.scs
(7). To print the schematic and the waveform to postscript file (.ps).
   - copy .cdsplotinit to work directory: cp /linux_apps/cadence/IC/tools/plot/etc/cdsplotinit .cdsplotinit
   - When plot in schematic window or hardcopy in waveform window, choose postscript output.
Start Cadence Tool

Command Interpreter Window (CIW)
Library Manager

CIW: Tools -> Library Manager.
Library Manager -- View

- **schematic** - contains the logical design of the device.

- **symbol** - contains the symbol representation of the schematic.

- **layout** - contains the silicon-level representations of the transistors and wiring.

- **CdsSpice, HspiceS, Spectre, spectreS** – contain spice information for the element.

- **abstract** - contains an abstract representation of the layout for use by Cadence place and route software.

- **extracted** - contains layout connectivity for use by verification programs.

- **behavioral** – contains the VHDL description of the cell
Creating a New Cellview

In the CIW or library manager, select FILE – New – Cellview.

Create a new cellview from the Library Manager or CIW.

- Specify the library Name, Cell Name, View Name, and Tool to use. The path to the *cds.lib* file will appear in the form and is not editable.
- Modify the Tool field to create a layout, verilog, symbol, schematic, vhdl, or ahdl view.
Create your own Library

- Select Tools>Library Manager.
Create your own Library

- From Lib manager menu, select File>New>Library.
- Type library name, e.g. my_test. Then click Next to see “Technology file for new library” window, select “Attach to an existing techfile”, click OK. Then select “Sige5am”.
- Click my_test lib and select File>New>cell view. Name your own cell and make sure view name is “schematic” and tool is “Composer-schematic”. Then click OK, you will see schematic interface.
Contents of Schematic
Add instance to your schematic

- Select Add – Instance or the bindkey “I” to display the ADD Instance form.
- Parameter units, such as ohms are implicit.
- Select “pfet” “nfet” from sige5am lib. Select “vdc” “gnd” from “analogLib”.
- Use “w” to add a wire.
- Use hotkey “Q” to change the instance property. Set your Vdd DC voltage as 3.3V, your input DC voltage Vin as 0.2V.
Adding Component Instances

- Design components are generally instances of a symbol cellview and might be design primitives. Here are some properties associated with design component instances:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Example Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Library Name</td>
<td>analogLib</td>
</tr>
<tr>
<td>Cell Name</td>
<td>res</td>
</tr>
<tr>
<td>View Name</td>
<td>symbol</td>
</tr>
<tr>
<td>Instance Name</td>
<td>R2</td>
</tr>
</tbody>
</table>

The Instance Name is assigned automatically, unless explicitly specified.

Find analog design primitives in the analogLib library. This library is included wherever the Analog Artist software is installed in the path ../tools/dfII/etc/cdslib/artist. Include this path in your library search path to use analogLib components.

The system prompts for component parameters when instantiating the components. Attach multiplier suffixes, such as k for 1000, to numerical quantities.

Use the rotate, upsidedown, and sideways buttons to change the orientation of your components as they are placed in the schematic.
Adding Source and Ground

Sources, taps, and grounds are instance of cells.
  Sample source cells are in the analog library.
  • Choose from independent, dependent, and place-wise linear (PWL) sources.
  • Choose tap and ground cells, which use to establish global nets.
  • An instance of the cell gnd is required in the design for DC convergence.
Adding Source and Ground

Adding Sources and Ground

- **Ground**
  Always include the symbol `gnd` found in the analogLib library. Analog simulators require that all nodes in the circuit must have a DC path ground. This would be represented as node 0 in the Cadence SPICE circuit simulator, for example. Use other ground symbols, such as `gnda`, for a ground that is connected to the reference ground through an analog circuit.

- **Voltage sources**
  Include all of your DC and transient voltage and current sources in the schematic. There are many types of voltage sources in analogLib. For example, some of the independent voltage sources are `vdc`, `vsin`, `vpulse`, `vexp`, `vpwl` and `vpwlf`. Each source has a current equivalent that begins with the letter `i`. There are also equivalent dependent sources.
  All sources generate input waveforms except for `pwlf` sources, which simulate a circuit using a text file of data tables. It is not necessary to include sources in the schematic, although this is often convenient. Attaching a stimulus file to the final netlist is discussed in the analog simulation section of this course.

- **Voltage taps**
  Use taps symbol to transfer voltages and currents throughout the design without using wires. Voltage tap symbols, such as `vcc`, `vdd`, `vcca`, and `vccd` are in the analogLib library.
Adding Pins

Pins have a user-defined Name and a Direction (input, output or input/output).

Pins are of three types:
- *Schematic* pins provide ports to a schematic.
- Symbol pins provide ports to a symbol representing a schematic, and are connection points to the symbol in a hierarchal design.
- Offsheet pins are used in large designs without hierarchy.

Pin names and directions must match in all cellviews of a cell.
Pins

For analog designers, pins have two primary functions:

- Pins represent connection points between different cellviews such as schematic, symbol, and layout representation. Using named pins identifies equivalent inputs, outputs, and I/O ports throughout the design environment.
- Pins provide connection points for objects which are hierarchically instantiated.

Pin Properties

Pins have a pin name, pin type, and pin direction. These should be consistent throughout your design.

Multiple Sheet Design with Offset Pins

The composer: Design Entry Help manual includes a section on multiple sheet design methodology and information on the offsheet pin type.

Pins (ipin, opin, iopin, sympin) now come from “basic” library.
Adding Wires and Wire Labels

Automatic routing is the default mode.

When not labeling a wire, the system names the net formed by the wires.

If the router cannot find a path between two points,

- A dotted “fight linw” is placed to establish connectivity only.
- Click on intermediate points to guide the router to yield a solid line of connectivity.
- Use the Cmd Options icon or F3 key to modify the wiring options.
Wires

Draw wires between the instance pins and schematic pins to connect them. Use wide wires to indicate multiple signals on a wire, the system does not force or check this. Draw wires at any angle, but most designers frequently restrain wires to orthogonal lines.

- Using Route Methodology
  The route draw mode chooses two points in your design and then it automatically routes a wire around components. If a routed net remains dotted, it is because there are no clear routing channel. This can happen if the instances are too close or overlap the selection boxes. To solve this, move the components further apart to give a routing channel.
  Routing method options exits to wire together two points immediately (the default) or indicate many points to route together later in a single step. More information on route methods is included in the design entry reference documentation.

- Wire Labels
  Labeling wires gives the corresponding net a meaningful name in the simulation results data. Otherwise nets are system named. There is some control over the automatically generated names, but these may not be meaningful as custom names.
  Click the **Cmd Options** icon in the schematic window or press the F3 key to change the default wiring setup.
Interconnecting Components

- Wire to Wire
- Wire to Pin
- Pin to Pin
- OUT
- IN
- OUT IN
- By Name (Local)
- VCCI
- Design Global Net

Schematic Pins and global symbol pins name wires by adoption.

Note: Inherited connections, not shown, will be discussed in the Inherited Connection chapter
Interconnecting Components

- **Physical Connectivity**
  All physical connections are made by wire to pin, wire to wire, or pin to pin connections.

- **Connectivity by Name**
  If two wires have been labeled with the same name, they become part of the same net when connectivity is established.

- **System Assigned Names**
  If a net is unnamed, the system generates a name such as net100 or net7. Optionally change the base name from net to something else. If a wire is connected to a schematic pin, then the pin is used to name the net by adoption when connectivity is established.

- **Global Nets**
  Any net or pin name that ends in an exclamation point will be part of a global net when connectivity is established. Global nets are automatically connected through the hierarchy without the use of wires. For example, voltage taps have symbol pin names that end in an exclamation point. If a wire is connected to a pin that has global name, the pin name is used to name the net by adoption. This is how voltage and ground signals are propagated throughout a design.
Schematic Checking

During schematic checking, all of the following are performed by default:

- **Update Connectivity**
  This process associates wires and pins with logical connections called nets.

- **Schematic Rules Check**
  - Logical checks
  - Physical checks
  - Name checks

- **Cross – View Checker**
  This option checks for pin name and direction consistency between cellviews.

Select **check – Rules setup** from a schematic window to edit the rules. Disable any or all of these schematic checking features, if not needed.
Schematic Checking

Schematic checking is a critical step in the design process. Either check a single cellview or descend through the hierarchy to check all cellviews in your design.

Checking a schematic accomplishes the following:

- **Update Connectivity** – When connectivity is established, wires and pins in the design entry window become associated with logical connections called nets. It is necessary to correct connectivity problems prior to going on to the next design phase.

- **Schematic Rules Check** – This process checks the schematic with a set of rules. Access them with the Check – Rules Setup command from the schematic window. The checks include:
  - Logical checks, such as Floating Input Pins and Shorted Output Pins.
  - Physical checks, such as Unconnected Wires and Overlapping Instances.
  - Name checks, such as Instances Name Syntax.

- **Cross-View Checker** – This option checks the pin consistency between different views of the cell. Pin name directions must match between cellviews.
Schematic Entry Flow

1. Open Design
2. Add Component Instances
3. Add Pins
4. Add and Name Wires
5. Check
6. Save
7. Symbol Editor
Simulator Setup

- Add the following files with correct order.
  - /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/definitions.scs
  - /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/design.scs
  - /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/process.scs

Chap 3, Cadence, 5190/6190, Foster Dai, 2013
Simulator Setup

- Another place for definition file
- /class/ibm_lib/5am/IBM_CDS/sige5am/relAM/models/spectre/definitions.scs
Simulate the circuit

- Select Analyses>Choose>DC
- Enable the DC analysis and save DC operating point
- Select Simulation>Netlist and Run. Then you will see a window pop-up and shows the simulation process.
Viewing simulation results

• Choose “Session”-> AWD for waveform viewer.
• From simulator, select Results>Annotate>DC node voltages and DC operating points. Then you will see the DC simulation results have been labeled in your schematic.
• You can select other analysis like “tran” and “ac” to verify your circuit’s functionality and performance.
• Usually Results>Direct Plot>Direct form command can give you a lot of simulation information you want.
Other Tools in Cadence Design Environment

**Virtuoso Composer** for schematic capture,

**Analog Environment** for simulation,

**Virtuoso Layout** for layout,

**Diva** for DRC (design rule checking),

**Diva** for extraction,

**Diva** for LVS (layout vs. schematic),

**Analog Environment** for postlayout simulation
DIVA Verification Tools

- Diva Design Rule Checker (DRC)
- Diva Layout vs. Schematic (LVS) Verifier (includes electrical rule checks (ERC) and extraction of device layout parameters)
- Diva Parasitic Extractor (RCX)
- Diva Physical Verification Suite (consists of Diva DRC and Diva LVS)
- Diva Physical Verification and Extractor Suite (consists of Diva DRC, Diva LVS, and Diva RCX)
# General Bindkey Chart

<table>
<thead>
<tr>
<th>Key</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z</td>
<td>Previous View</td>
</tr>
<tr>
<td>^v</td>
<td>Go To CIW</td>
</tr>
<tr>
<td>↓</td>
<td>Pan Down</td>
</tr>
<tr>
<td>←</td>
<td>Pan Left</td>
</tr>
<tr>
<td>→</td>
<td>Pan Right</td>
</tr>
<tr>
<td>↑</td>
<td>Pan Up</td>
</tr>
<tr>
<td>F3</td>
<td>Toggle Options Form</td>
</tr>
<tr>
<td>F4</td>
<td>Toggle Partial Selection</td>
</tr>
<tr>
<td>r</td>
<td>Rotate (EF)</td>
</tr>
<tr>
<td>R</td>
<td>Sideways (EF)</td>
</tr>
<tr>
<td>^r</td>
<td>Upside Down (EF)</td>
</tr>
<tr>
<td>Del</td>
<td>Undo Point (EF), Delete</td>
</tr>
<tr>
<td>Esc</td>
<td>Stop Command Iteration</td>
</tr>
<tr>
<td>F1</td>
<td>Help</td>
</tr>
<tr>
<td>Help</td>
<td>Help</td>
</tr>
</tbody>
</table>

**VERILOG HDL or VHDL**

<table>
<thead>
<tr>
<th>Key</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>^s</td>
<td>Save As</td>
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<tr>
<td>^e</td>
<td>Return</td>
</tr>
<tr>
<td>Esc</td>
<td>Check and Save</td>
</tr>
<tr>
<td>S</td>
<td>Search</td>
</tr>
<tr>
<td>Open</td>
<td></td>
</tr>
<tr>
<td>Print</td>
<td></td>
</tr>
<tr>
<td>Return To Top</td>
<td></td>
</tr>
<tr>
<td>Close Window</td>
<td></td>
</tr>
</tbody>
</table>
Mouse Buttons Bindkey Chart

**Left Mouse Button – Select and Deselect**
- Click: Select Point
- Double Click: Extend Select
- Shift Click: Select Point (Add)
- Cntl Click: Deselect Point
- Drawthrough: Select Box or Direct Edit*
- Shift Drawthrough: Select Box (Add) or Direct Edit*
- Cntl Drawthrough: Deselect Box or Direct Edit*
- Click (EF): Add Point

*Direct Edit applies only when over object.

**Middle Mouse Button – Pop-Up Menus**
- Click: Pop-Up Menus
- Click (EF): Pop-Up Menus
- Double Click (EF): Toggle Options Form

**Right Mouse Button – Repeat, Zoom, Options**
- Click: Repeat Last Command
- Drawthrough: Zoom In
- Shift Drawthrough: Zoom Out
- (EF): Command Options
Schematic Editor Bindkey Chart

**DESIGN**
- X  Check and Save
- S  Save (not needed)
- ^s  Save As
- E  Hierarchy–Descend Edit
- e  Hierarchy–Descend Read
- Hierarchy–Edit In Place
- Hierarchy–Show Scope
- ^e  Hierarchy–Return
- Hierarchy–Return To Top
- Create Cellview
- New
- Open
- Discard Edits
- Make Read Only
- Make Editable
- g  Probe–Add Net
- /  Renumber Instances

**WINDOW**
- z  Zoom In
- ]  Zoom In By 2
- ↓  Pan Down
- ←  Pan Left
- →  Pan Right
- ↑  Pan Up
- f  Fit
- F6  Redraw
- Utilities
- Close

**EDIT**
- u  Undo
- U  Redo
- m  Stretch
- c  Copy
- M  Move
- Del  Delete
- r  Rotate
- q  Properties–Objects
- Properties–Cellviews
- Q  Reset Invisible Labels
- Component Display
- Alternate View
- ^f  Select–Filter
- Search
- 5  Route Flight

**ADD**
- i  Instance
- w  Wire (narrow)
- W  Wire (wide)
- l  Wire Name
- p  Pin
- b  Block
- Net Expression
- Solder Dot
- L  Note–Text
- n  Note–Shape

**CHECK**
- x  Current Cellview
- Hierarchy
- Options
- Rules Setup
- Label Attachment
- Find Marker
- Delete Marker
- Delete All Markers
- Simulation Monitors

**OPTIONS**
- O  Editor
- Display
- ^f  Select Filter
- Check
- Check Rules Setup
- Parameter Filter
- Save Defaults
- Load Defaults
Symbol Editor Bindkey Chart

<table>
<thead>
<tr>
<th>DESIGN</th>
<th>WINDOW</th>
<th>EDIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>u</td>
</tr>
<tr>
<td>S</td>
<td>Save (not needed)</td>
<td>U</td>
</tr>
<tr>
<td>^s</td>
<td>Save As</td>
<td>m</td>
</tr>
<tr>
<td>E</td>
<td>Hierarchy–Descend Edit</td>
<td>c</td>
</tr>
<tr>
<td>e</td>
<td>Hierarchy–Descend Read</td>
<td>M</td>
</tr>
<tr>
<td></td>
<td>Hierarchy–Edit In Place</td>
<td>Del</td>
</tr>
<tr>
<td></td>
<td>Hierarchy–Show Scope</td>
<td>r</td>
</tr>
<tr>
<td>^ e</td>
<td>Hierarchy–Return</td>
<td>q</td>
</tr>
<tr>
<td></td>
<td>Hierarchy–Return To Top</td>
<td>Properties–Objects</td>
</tr>
<tr>
<td>g</td>
<td>Create Cellview</td>
<td>Q</td>
</tr>
<tr>
<td></td>
<td>New</td>
<td>Utilities</td>
</tr>
<tr>
<td></td>
<td>Open</td>
<td>^ f</td>
</tr>
<tr>
<td></td>
<td>Discard Edits</td>
<td>Origin</td>
</tr>
<tr>
<td></td>
<td>Make Read Only</td>
<td>Search</td>
</tr>
<tr>
<td></td>
<td>Make Editable</td>
<td></td>
</tr>
<tr>
<td>g</td>
<td>Probe–Add Net</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Plot</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ADD</th>
<th>CHECK</th>
<th>OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>Pin</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td>Shape</td>
<td>Editor</td>
</tr>
<tr>
<td>l</td>
<td>Label</td>
<td>o</td>
</tr>
<tr>
<td></td>
<td>Selection Box</td>
<td>Display</td>
</tr>
<tr>
<td>L</td>
<td>Note → Text</td>
<td>^ f</td>
</tr>
<tr>
<td>n</td>
<td>Note → Shape</td>
<td>Select Filter</td>
</tr>
<tr>
<td></td>
<td>Net Expression</td>
<td>Save Defaults</td>
</tr>
<tr>
<td></td>
<td>Custom Pin</td>
<td>Load Defaults</td>
</tr>
<tr>
<td></td>
<td>Import Symbol</td>
<td></td>
</tr>
</tbody>
</table>
# Layout Bindkey Map

## F keys

<table>
<thead>
<tr>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>F4</th>
<th>F5</th>
<th>F6</th>
<th>F7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Help</td>
<td>Save</td>
<td>Toggle Partial Select</td>
<td>Open Design</td>
<td>Maintain Connections</td>
<td>Guided Path</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>F8</th>
<th>F9</th>
<th>F10</th>
<th>F11</th>
<th>F12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Guided Path Create</td>
<td>Filter Size</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Alphabet keys

Key to Map: 1=Top row is Control + key  
2=Middle row is Shift + key  
3=Bottom row is key

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Select All</td>
<td>1</td>
<td>1 Interrupt</td>
<td>1 Deselect All</td>
<td>1</td>
</tr>
<tr>
<td>2 Select Area</td>
<td>2 Return</td>
<td>2 Chop</td>
<td>2 Deselect Area</td>
<td>2 Display Ops.</td>
</tr>
<tr>
<td>3 Select</td>
<td>3 Go to Level</td>
<td>3 Copy</td>
<td>3 Deselect</td>
<td>3 Edit Options</td>
</tr>
<tr>
<td>F</td>
<td>G</td>
<td>H</td>
<td>I</td>
<td>J</td>
</tr>
<tr>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----------------------</td>
<td>-----</td>
</tr>
<tr>
<td>1 View 0</td>
<td>1</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2 View 32</td>
<td>2</td>
<td>Zoom To Grid</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3 Fit All</td>
<td>3</td>
<td>Toggle Gravity</td>
<td>3 Create Instance</td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>L</td>
<td>M</td>
<td>N Snap mode options:</td>
<td>O</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1 diagonal</td>
<td>1</td>
</tr>
<tr>
<td>2 Clear Rulers</td>
<td>2</td>
<td>Merge</td>
<td>2 orthogonal</td>
<td>2 Rotate</td>
</tr>
<tr>
<td>3 Draw Rulers</td>
<td>3</td>
<td>Label</td>
<td>3 Move</td>
<td>3 L90XFirst</td>
</tr>
<tr>
<td>P</td>
<td>Q</td>
<td>R</td>
<td>S</td>
<td>T</td>
</tr>
<tr>
<td>1 Create Pin</td>
<td>1</td>
<td>Redraw</td>
<td>1 Split</td>
<td>1 Zoom to Set</td>
</tr>
<tr>
<td>2 Create Polygon</td>
<td>2</td>
<td>Design Prop</td>
<td>2 Reshape</td>
<td>2 Search</td>
</tr>
<tr>
<td>3 Create Path</td>
<td>3</td>
<td>Object Prop</td>
<td>3 Create Rectangle</td>
<td>3 Stretch</td>
</tr>
<tr>
<td>U</td>
<td>V</td>
<td>W</td>
<td>X</td>
<td>Y</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Type In GIW</td>
<td>1 Close</td>
<td>1 Fit Edit</td>
</tr>
<tr>
<td>2 Redo</td>
<td>2</td>
<td>Next View</td>
<td>2 Descend</td>
<td>2 Paste</td>
</tr>
<tr>
<td>3 Undo</td>
<td>3</td>
<td>Attach</td>
<td>3 Previous View</td>
<td>3 Edit-In-Place</td>
</tr>
<tr>
<td>Z</td>
<td>Esc</td>
<td>Tab</td>
<td>Delete</td>
<td>Back Space</td>
</tr>
<tr>
<td>1 Zoom In x2</td>
<td>Cancel</td>
<td>Pan</td>
<td>Delete</td>
<td>Undo Point</td>
</tr>
<tr>
<td>2 Zoom out x2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 Zoom In</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Return</td>
<td>Enter last point</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Chap 3, Cadence, 5190/6190, Foster Dai, 2013
## Layout Bindkey Map

### Arrow keys
- **Control + key**: Fit cell to portion of window
- **Shift + key**: Move Cursor
- **Key**: Pan to portion of cellview

<table>
<thead>
<tr>
<th>R7 Home up left</th>
<th>R8 top</th>
<th>R9 PgUp up right</th>
</tr>
</thead>
<tbody>
<tr>
<td>R10 left</td>
<td>R11 center</td>
<td>R12 right</td>
</tr>
<tr>
<td>R13 End down left</td>
<td>R14 bottom</td>
<td>R15 PgDn down right</td>
</tr>
</tbody>
</table>

### Symbol keys on arrow key pad

<table>
<thead>
<tr>
<th>= R4</th>
<th>/ R5</th>
<th>* R6</th>
<th>-</th>
<th>+</th>
<th>Enter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Moves cursor .5 grid points when used with Shift and arrow keys</td>
<td>Moves cursor 1 grid point when used with Shift and arrow keys</td>
<td>Moves cursor 2 grid points when used with Shift and arrow keys</td>
<td>Delete reference point</td>
<td>Set reference point</td>
<td>Enter point</td>
</tr>
</tbody>
</table>
Differential Current Mode Logic

Same CML circuit topology/layout for AND/OR/NAND/NOR with only different input/output polarities

Chap 3, Cadence, 5190/6190, Foster Dai, 2013
CML latch with active low reset using 4-level transistors

![CML latch diagram]

Chap 3, Cadence, 5190/6190, Foster Dai, 2013
Bias for Current Mode Logic

3.3V

Choose load res with mim W=2μm to lower the load capacitance

3.1V

Output bias at 3.1V
Diff swing=424mVc

2.2V

Adding diodes to prevent breakdown and balance the diff pair bias

1.3V

Leimit=1μm
Peak fT current=603μA

Vref from bandgap ref optimized for const. VS

Choose W=4μm, m=3 for better res accuracy

Bias current=400μA
Level Shifter for Current Mode Logic

Bias Current can be tuned for different drive strength

Lemit=1μm
Peak $f_T$ current=603μA

Bias Current can be tuned for different drive strength

Choose MOSFET for better current mirror accuracy and less headroom

Bias current=400μA
A Divided-By-2 Circuit

Diagram:

Input: $D$, $CLK$

Output: $Q$, $\overline{Q}$

Waveforms:

Input = $CLK$

$D = \overline{Q}$

Output = $Q$

$0$

Equations:

Input = $CLK$

$D = \overline{Q}$

Output = $Q$

0
Master-Slave D Flip-Flop

(a) (clock)
Current Mode Master-Slave D-Flip-Flop w. EF

EF can be inserted to prevent saturation; needs higher supply voltage
• Use minimum size npn transistors with Lemit=1um to design the following CML circuit:

• (1) 5130/6130: differential AND gate (left);
• (2) 6130 only: Divided by 2 circuit (right);

Project report due on **Oct. 22**, Email your report in **yourname_proj2.doc** format to **daifa01@auburn.edu**. Report includes schematics and Cadence transient simulation results for input/output waveforms showing the maximum operation frequency.
Copy Cadence Schematic and Waveform to Word

1. Copy .cdsplotinit to your launch directory. In schematic window, Choose “design → plot → deselect header → plot options → plotter name → send plot only to file”. In waveform window, Choose “hardcopy → deselect header → plotter name → send plot only to file”. It will generate a ps file in the specified directory.

2. You may also do printscreen. After editing it with MS Paint, you need to save it as .jpg format instead of the default .bmp format. Then you can insert the .jpg file in the word document using Insert --> Picture --> From File option. This way, the size of the .jpg file is approximately 30KB.

3. Another way is to use GhostView, GhostScript softwares to get the .jpg files. These softwares can be downloaded from: http://www.cs.wisc.edu/~ghost/doc/AFPL/get811.htm

4. In Cadence, you can get .ps file by selecting the Tools on the Command Interpreter Window and then Camera --> PostScript then select the window to get the .ps file. (you need to wait for sometime until the process is complete). This .ps file is opened with the ghostview software and converted into a .jpg format file which is later used in the word document as explained above.

5. Do your best to minimize the file size for your report.