ELEC 5780/6780, Section 001, Fall 2015
Broun Hall 235, Tuesday and Thursday 3:30-4:45pm

Analog Circuit Design

By

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Chapter 4

Cadence® Analog Design Environment

- Getting started with Cadence Tool
- Schematic Editor
- Project

Cadence tool information @

http://www.cadence.com/datasheets/

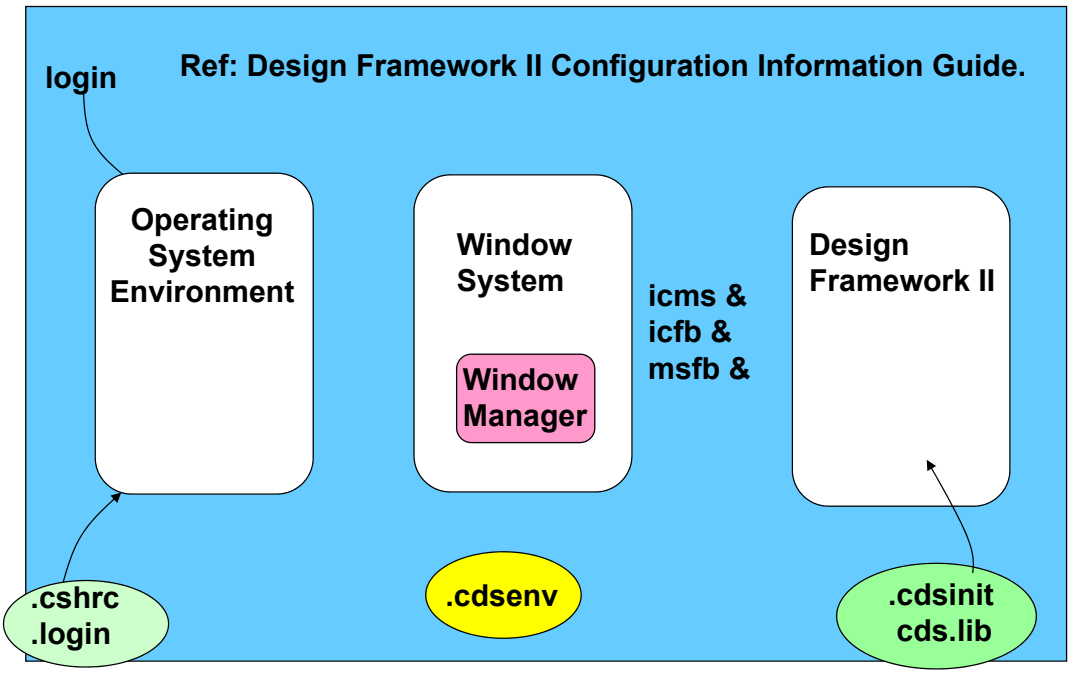
It supports RF/Analog and mixed-signal simulation

Getting Started

- Install cadence tool: under UNIX, user services → user setup → Electronics Data Analysis (EDA) → eda/cadence/1.0
- Setup cadence tool and PDK lib: under UNIX, mkdir Name6780, place .cdsenv, .cdsinit, .cdsplotinit and cds.lib to Name6780.
- Add the following in your .cshrc file (see sample_cshrc file):

  setenv CDS_Netlisting_Mode "Analog "
- Launch Cadence: in "Name6780" by typing icfb& or icms& or msfb
- Cadence Manu: pdf files @ /opt/cadence/ic4.46/doc, use help or type "openbook&" under UNIX.

Design System Initialization Files



Required Software

Cisco AnyConnect VPN:
http://www.auburn.edu/oit/vpn/

PuTTY:
http://the.earth.li/~sgtatham/putty/0.63/x86/putty.exe

VNC Viewer:
https://www.realvnc.com/download/viewer/

Cisco

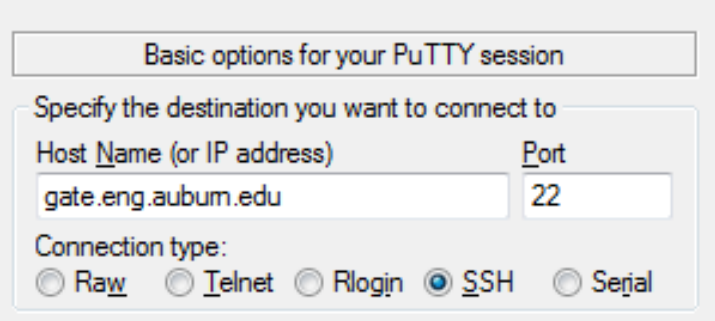
Type host name and connect:

PuTTY

1.Hostname:gate.eng.auburn.edu

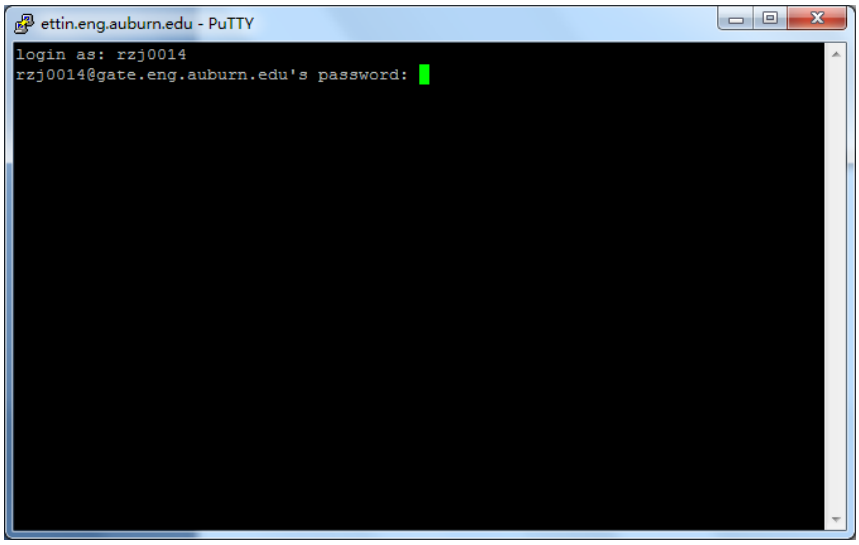
2.Port:22

3.Check “SSH”.



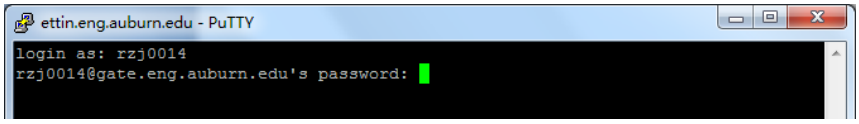
PuTTY

- 4. Log in with user name and pass word

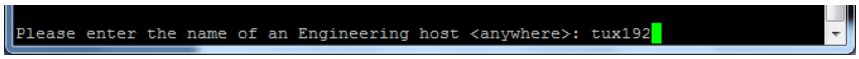


PuTTY

5. Log in with user name and pass word0



6. Type the tux name (Like here, tux192)



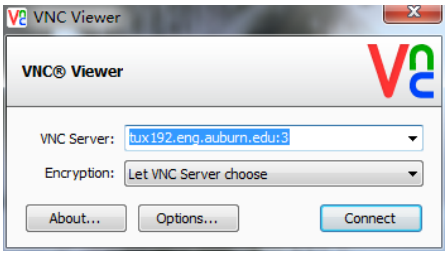
7. After reenter the password, type:
vncserver -depth 24 -geometry 1366x768

8. Record this line for vnc viewer:

```
tux192.eng.auburn.edu:3
```

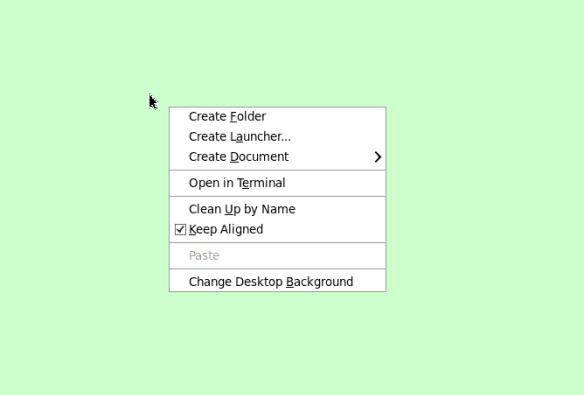

VNC Viewer

1. Type the server which recorded from PuTTY



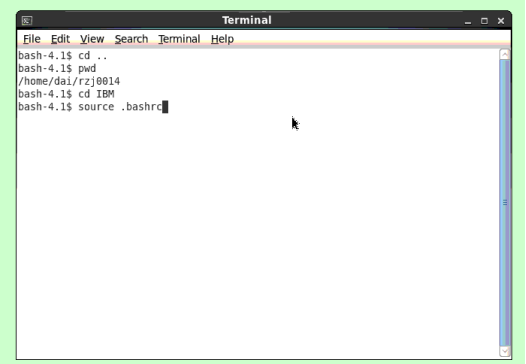
VNC Viewer

2. After putting all your setup up files in one folder, right click mouse, and click open in terminal.



VNC Viewer

3. Copy the class-provided .bashrc file to your home directory ("~" is your home directory).
4. Type "source .bashrc" when you are under home directory.



5.Type icfb to enter cadence IC5.

Design System Initialization Files

- **.bashrc or** .cshrc and .login → configure the operating system environment and the UNIX environment when you login and start a UNIX application. (Linux environment is preferred)
- .cdsinit → customizes the Affirma Analog Circuit Design Environment.
- .cdsenv → configure Cadence Analog Artist tool environment.
- cds.lib → set paths to the libraries used by the Analog Artist software.

  Cadence default lib:

  INCLUDE /linux_apps/cadence/IC/share/cdssetup/cds.lib

  User defined lib:

  DEFINE Dai6970 ~/elec6190/Dai6970
- Cadence process design kit (PDK) can be downloaded www.cadencePDK.com

Start Cadence Tool

- **icfb&** → front to back design,
  default CDS_Netlisting_Mode “Digital“
- **icms&** → mixed signal design,
  default CDS_Netlisting_Mode “Digital“
- **msfb&** → mixed signal front to back design,
  default CDS_Netlisting_Mode “Analog“, don’t need to add setenv CDS_Netlisting_Mode "Analog “ in **.bashrc or** .cshrc.
- Schematic cellview to cellview defaults for creating a symbol with Artist. The default is to not create an Artist symbol.

  The following has been added in .cdsinit:

  schSetEnv("tsgTemplateType" "artist")

Initializing Design Framework II Environment

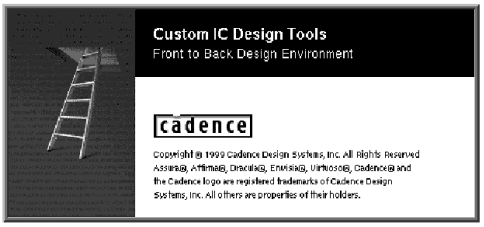
The Design Framework II software reads your *.cdsinit* file at startup to set up your environment.

.cdsinit:
Sets user-defined bindkeys.
Redefines system-wide defaults.
Contains SKILL commands.

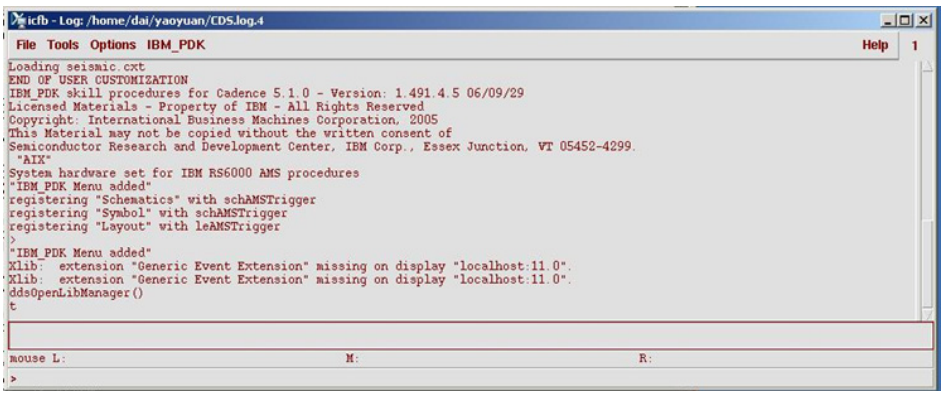
The search order for the *.cdsinit* file is:
<Filename><install_dir>/tools/dfII/*local*
the current directory [Name6970] ← put .cdsenv, .cdsinit, cds.lib here
the home directory
When a .cdsinit file is found, the search stops unless a command in *.cdsinit* reads other files.

Path to a sample .cdsinit file:
<Filename><install_dir>/tools/dfII/samples/artist/cdsinit
<install_dir>=/opt/cadence/ic5.033

Start Cadence Tool

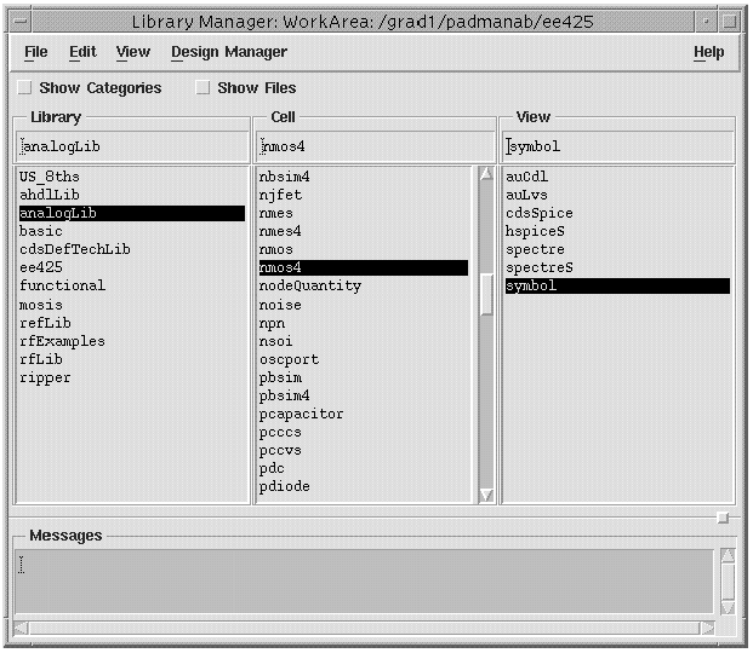


Command Interpreter Window (CIW)



Library Manager

CIW: Tools -> Library Manager.



Library Manager -- View

- ***schematic*** - contains the logical design of the device.
- ***symbol*** - contains the symbol representation of the schematic.
- ***layout*** - contains the silicon -level representations of the transistors and wiring.
- ***CdsSpice***, ***HspiceS***, ***Spectre***, ***spectreS*** –contain spice information for the element.
- ***abstract*** - contains an abstract representation of the layout for use by Cadence place and route software.
- ***extracted*** - contains layout connectivity for use by verification programs.
- ***behavioral*** – contains the VHDL description of the cell

Creating a New Cellview

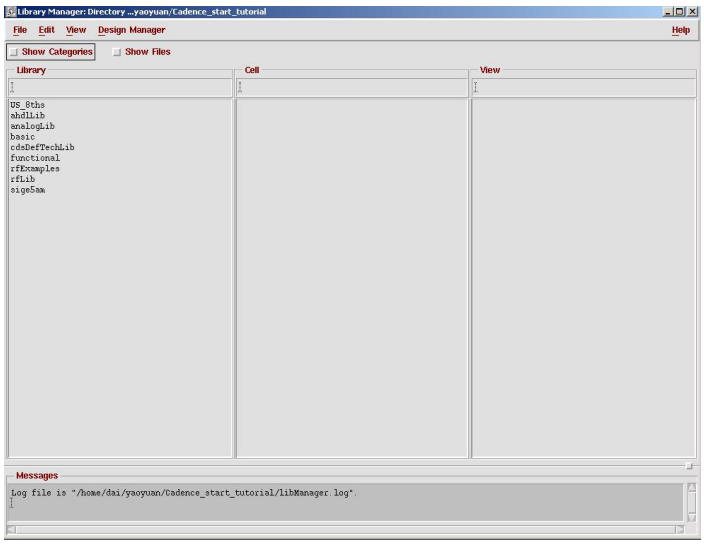
In the CIW or library manager, select FILE – New – Cellview.

Create a new cellview from the Library Manager or CIW.

- Specify the library Name, Cell Name, View Name, and Tool to use. The path to the *cds.lib* file will appear in the form and is not editable.
- Modify the Tool field to create a layout, verilog, symbol, schematic, vhdl, or ahdl view.

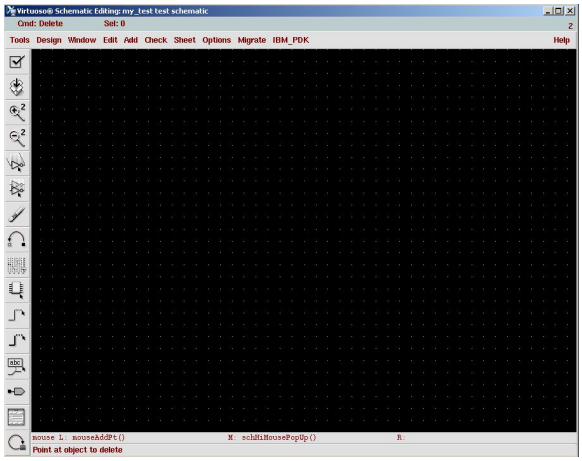
Creat your own Library

- Select Tools>Library Manager.

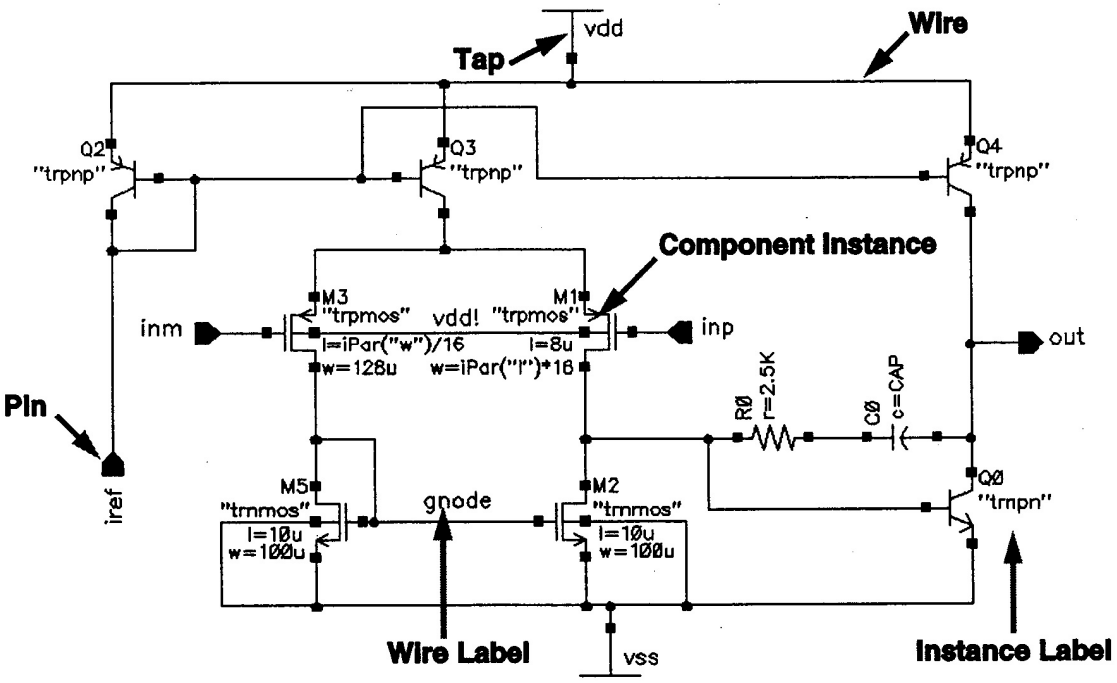


Creat your own Library

- From Lib manager menu, select File>New>Library.
- Type library name, e.g. my_test. Then click Next to see “Technology file for new library” window, select “Attach to an existing techfile”, click OK. Then select “PDK”.
- Click my_test lib and select File>New>cell view. Name your own cell and make sure view name is “schematic” and tool is “Composer-schematic”. Then click OK, you will see schematic interface.

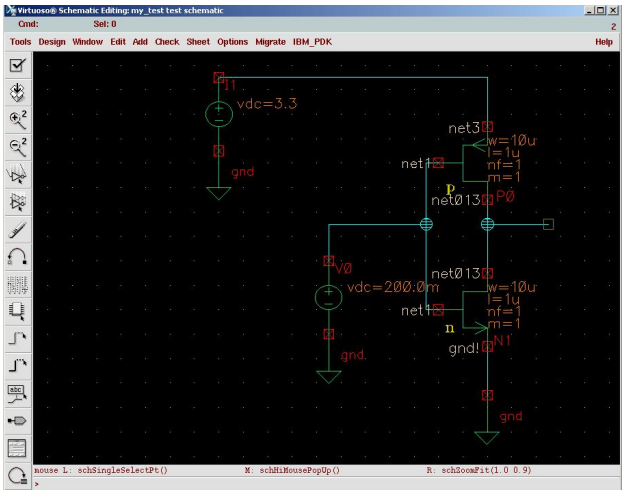


Contents of Schematic



Add instance to your schematic

- Select Add – Instance or the bindkey “I” to display the ADD Instance form.
- *Parameter units, such as ohms are implicit.*
- Select “pfet” “nfet” from PDK lib. Select “vdc” “gnd” from “analogLib”.
- Use “w” to add a wire.
- Use hotkey “Q” to change the instance property. Set your Vdd DC voltage as 3.3V, your input DC voltage Vin as 0.2V.



Adding Component Instances

- **Design components are generally instances of a symbol cellview and might be design primitives. Here are some properties associated with design component instances:**

Parameter	Example Value
Library Name	analogLib
Cell Name	res
View Name	symbol
Instance Name	R2

The Instance Name is assigned automatically, unless explicitly specified.

Find analog design primitives in the analogLib library. This library is included wherever the Analog Artist software is installed in the path *../tools/dfII/etc/cdslib/artist*. Include this path in your library search path to use analogLib components.

The system prompts for component parameters when instantiating the components. Attach multiplier suffixes, such as k for 1000, to numerical quantities.

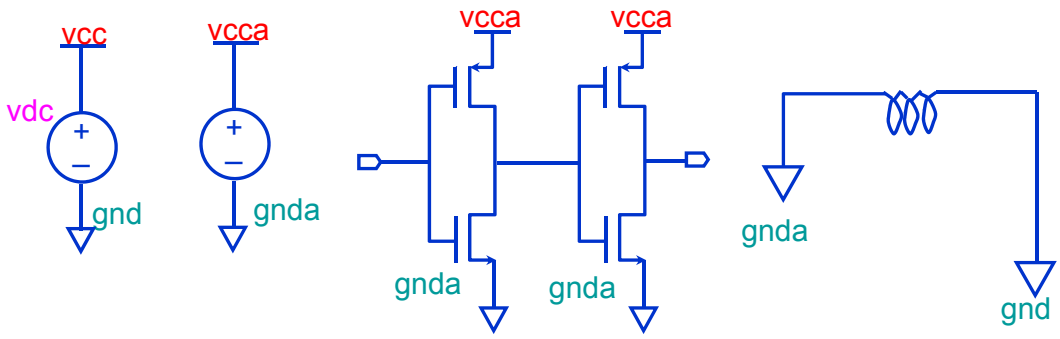
Use the rotate, upsidedown, and sideways buttons to change the orientation of your components as they are placed in the schematic.

Adding Source and Ground

Sources, taps, and grounds are instance of cells.

Sample source cells are in the *analog library*.

- Choose from independent, dependent, and place-wise linear (PWL) sources.
- Choose tap and ground cells, which use to establish global nets.
- An instance of the cell gnd is required in the design for DC convergence.



Adding Source and Ground

Adding Sources and Ground

- **Ground**

  Always include the symbol gnd found in the analogLib library, Analog simulators require that all nodes in the circuit must have a DC path ground. This would be represented as node 0 in the Cadence SPICE circuit simulator, for example. Use other ground symbols, such as gnda, for a ground that is connected to the reference ground through an analog circuit.

- **Voltage sources**

  Include all of your DC and transient voltage and current sources in the schematic, There are many types of voltage sources in analogLib. For example, some of the independent voltage sources are *vdc*, *vsin*, *vpulse*, *vexp*, *vpwl* and *vpwlf*. Each source has a current equivalent that begins with the letter i. There are also equivalent dependent sources.

  All sources generate input waveforms except for pwlf sources, which simulate a circuit using a text file of data tables. It is not necessary to include sources in the schematic, although this is often convenient. Attaching a stimulus file to the final netlist is discussed In the analog simulation section of this course.

- **Voltage taps**

  Use taps symbol to transfer voltages and currents throughout the design without using wires. Voltage tap symbols, such as *vcc,vdd,vcca*, and *vccd* are in the analogLib library.

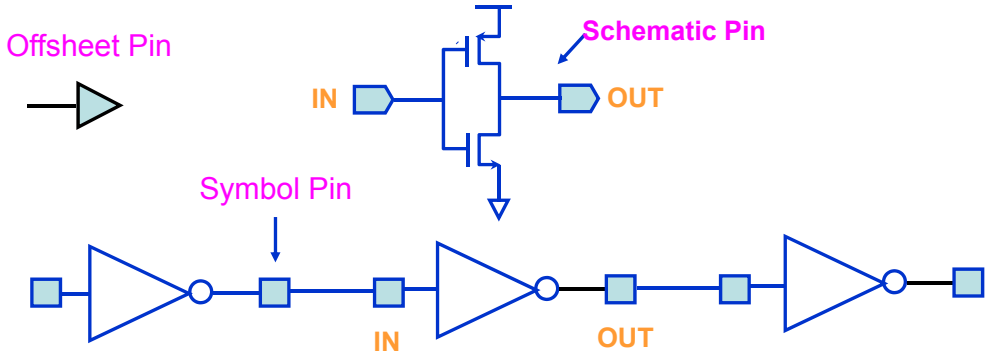
Adding Pins

Pins have a user-defined Name and a Direction (input, output or input/output).

Pins are of three types:

- *Schematic* pins provide ports to a schematic.
- Symbol pins provide ports to a symbol representing a schematic, and are connection points to the symbol in a hierarchal design.
- Offsheet pins are used in large designs without hierarchy.

Pin names and directions must match in all cellviews of a cell.



Pins

For analog designers, pins have two primary functions:

- Pins represent connection points between different cellviews such as schematic, symbol, and layout representation. Using named pins identifies eqivalent inputs, outputs, and I/O ports throughout the design environment.
- Pins provide connection points for objects which are hierarchically instantiated.

Pin Properties

Pins have a pin name, pin type, and pin direction. These should be consistent throughout your design.

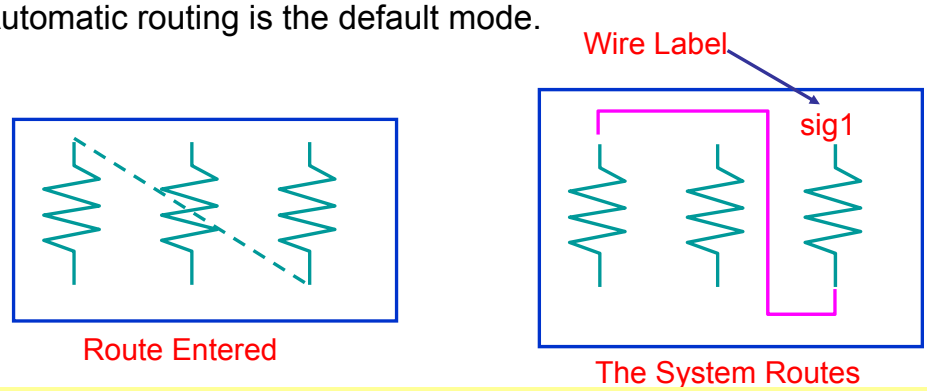
Multiple Sheet Design with Offset Pins

The composer: Design Entry Help manual includes a section on multiple sheet design methodology and information on the offsheet pin type.

Pins (***ipin, opin, iopin, sympin***) now come from “basic” library.

Adding Wires and Wire Labels

Automatic routing is the default mode.



When not labeling a wire, the system names the net formed by the wires.

If the router cannot find a path between two points,

• Adotted “fight linw” is placed to establish connectivity only.

•Click on intermediate points to guide the router to yield a solid line of connectivity.

•Use the Cmd Options icon or F3 key to modify the wiring options.

Wires

Draw wires between the instance pins and schematic pins to connect them. Use wide wires to indicate multiple signals on a wire, the system does not force or check this. Draw wires at any angle, but most designers frequently restrain wires to orthogonal lines

- **Using Route Methodology**

  The route draw mode chooses two points in your design and then it automatically routes a wire around components. If a routed net remains dotted, it is because there are no clear routing channel. This can happen if the instances sre too close or overlap the selection boxes. To solve this, move the components further apart to give a routing channel.

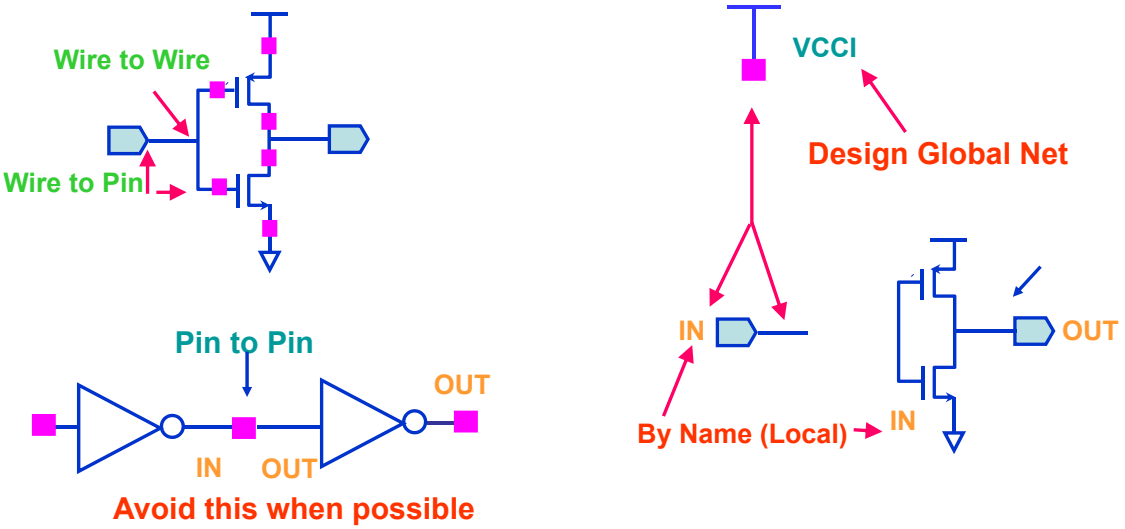
  Routing method options exits to wire together two points immediately (the default) or indicate many points to route together later in a single step. More information on route methods in included in the design entry reference documentation.

- **Wire Labels**

  Labeling wires gives the corresponding net a meaningful name in the simulation results data. Otherwise nets are system named. There is some control over the automatically generated names, but these may not be meaningful as custom names

  Click the Cmd Options icon in the schematic window or press the F3 key to change the default wiring setup.

Interconnecting Components



Schematic Pins and glabal symbol pins name wires by adoption.

Note: Inherited connections, not shown, will be discussed in the Inherited Connection chapter

Interconnecting Components

- **Physical Connectivity**
  All physical connections are made by wire to pin, wire to wire, or pin to pin connections.
- **Connectivity by Name**
  If two wires have been labeled with the same name, they become part of the same net when connectivity is established.
- **System Assigned Names**
  If a net is unnamed, the system generates a name such as net100 or net7. optionally change the base name from net to something else. If a wire is connected to a schematic pin, then the pin is used to name the net by adoption when connectivity is established,
- **Global Nets**
  Any net or pin name that ends in an exclamation point will be part of a global net when connectivity is established. Global nets are automatically connected through the hierarchy without the use of wires. For example, voltage taps have symbol pin names that end in an exclamation point. If a wire is connected to a pin that has global name, the pin name is used to name the net by adoption. This is how voltage and ground signals are propagated throughout a design.

Schematic Checking

During schematic checking, all of the following are performed by default:

- Update Connectivity

  This process associates wires and pins with logical connections called nets.
- Schematic Rules Check

  - Logical checks

  - Physical checks

  - Name checks
- Cross – View Checker

  This option checks for pin name and direction consistency between cellviews.

  Select **check** – **Rules setup** from a schematic window to edit the rules. Disable any or all of these schematic checking features, if not needed.

Schematic Checking

Schematic checking is a critical step in the design process.

Either check a single cellview or descend through the hierarchy to check all cellviews in your design.

Checking a schematic accomplishes the following:

- **Update Connectivity – When connectivity is established, wires and pins in the design entry window become associated with logical connections called nets. It is necessary to correct connectivity problems prior to going on to the next design phase.**
- **Schematic Rules Check – This process checks the schematic with a set of rules. Access them with the Check – Rules Setup command from the schematic window.**

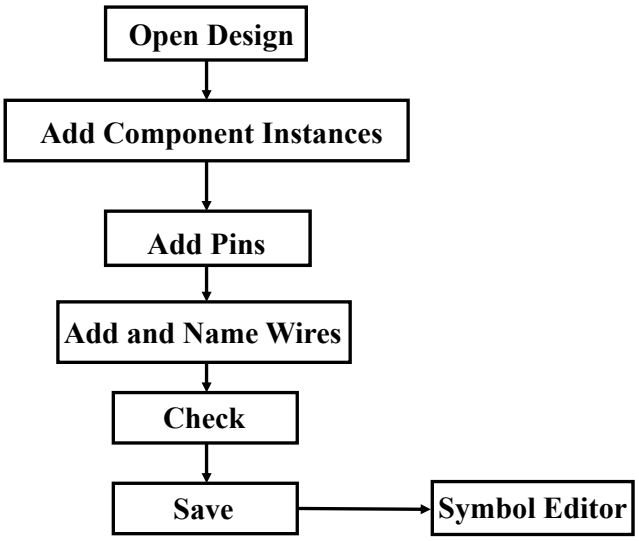
  The checks include:

  -- Logical checks, such as Floating Input Pins and Shorted Output Pins.

  -- Physical checks, such as Unconnected Wires and Overlapping Instances.

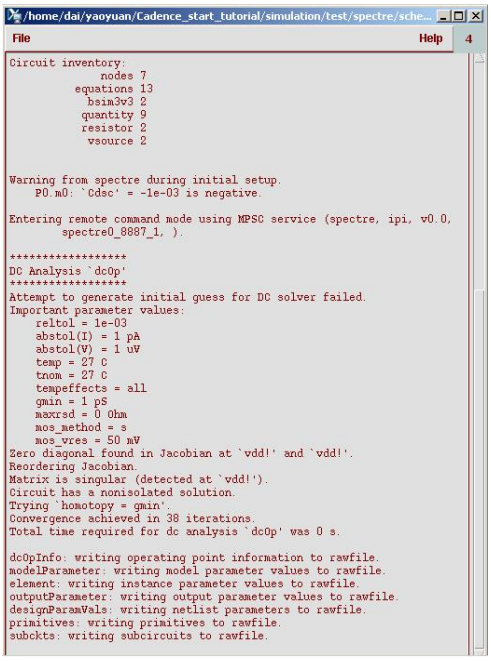
  -- Name checks, such as Instances Name Syntax.
- **Cross-View Checker – This option checks the pin consistency between different views of the cell. Pin name directions must match between cellviews.**

Schematic Entry Flow



Simulate the circuit

- Select Analyses>Choose>DC
- Enable the DC analysis and save DC operating point
- Select Simulation>Netlist and Run. Then you will see a window pop-up and shows the simulation process.



Viewing simulation results

- Choose “Session”-> AWD for waveform viewer.
- From simulator, select Results>Annotate>DC node voltages and DC operating points. Then you will see the DC simulation results have been labeled in your schematic.
- You can select other analysis like “tran” and “ac” to verify your circuit’s functionality and performance.
- Usually Results>Direct Plot>Main form command can give you a lot of simulation information you want.

Other Tools in Cadence Design Environment

Virtuoso Composer for schematic capture,

Analog Environment for simulation,

Virtuoso Layout for layout,

Diva for DRC (design rule checking),

Diva for extraction,

Diva for LVS (layout vs. schematic),

Analog Environment for postlayout simulation

DIVA Verification Tools

- **Diva Design Rule Checker (DRC)**
- **Diva Layout vs. Schematic (LVS) Verifier (includes electrical rule checks (ERC) and extraction of device layout parameters)**
- **Diva Parasitic Extractor (RCX)**
- **Diva Physical Verification Suite (consists of Diva DRC and Diva LVS)**
- **Diva Physical Verification and Extractor Suite (consists of Diva DRC, Diva LVS, and Diva RCX)**

General Bindkey Chart

Z	Previous View
^ v	Go To CIW
↓	Pan Down
←	Pan Left
→	Pan Right
↑	Pan Up
F3	Toggle Options Form
F4	Toggle Partial Selection
r	Rotate (EF)
R	Sideways (EF)
^ r	Upside Down (EF)
Del	Undo Point (EF), Delete
Esc	Stop Command Iteration
F1	Help
Help	Help

VERILOG HDL or VHDL

	Check and Save
^ s	Save As
	Search
	Open
	Print
^ e	Return
	Return To Top
	Close Window

Mouse Buttons Bindkey Chart

Left Mouse Button – Select and Deselect
Click Select Point
Double ClickExtend Select
Shift ClickSelect Point (Add)
Cntl ClickDeselect Point
DrawthroughSelect Box or Direct Edit*
Shift DrawthroughSelect Box (Add) or Direct Edit*
Cntl DrawthroughDeselect Box or Direct Edit*
Click (EF)Add Point

*Direct Edit applies only when over object.

Middle Mouse Button – Pop-Up Menus
Click Pop-Up Menus
Click (EF)Pop-Up Menus
Double Click (EF)Toggle Options Form

Right Mouse Button – Repeat, Zoom, Options
Click Repeat Last Command
DrawthroughZoom In
Shift DrawthroughZoom Out
(EF) Command Options

Schematic Editor Bindkey Chart

	DESIGN
X	Check and Save
S	Save (not needed)
^ s	Save As
E	Hierarchy–Descend Edit
e	Hierarchy–Descend Read
	Hierarchy–Edit In Place
	Hierarchy–Show Scope
^ e	Hierarchy–Return
	Hierarchy–Return To Top
	Create Cellview
	New
	Open
	Discard Edits
	Make Read Only
	Make Editable
9	Probe–Add Net
	Plot
/	Renumber Instances

	WINDOW
z	Zoom In
]	Zoom In By 2
[	Zoom Out By 2
↓	Pan Down
←	Pan Left
→	Pan Right
↑	Pan Up
f	Fit
F6	Redraw
	Utilities
	Close

	EDIT
u	Undo
U	Redo
m	Stretch
c	Copy
M	Move
Del	Delete
r	Rotate
q	Properties–Objects
Q	Properties–Cellviews
	Reset Invisible Labels
	Component Display
	Alternate View
^ f	Select–Filter
	Search
5	Route Flight

	ADD
i	Instance
w	Wire (narrow)
W	Wire (wide)
l	Wire Name
p	Pin
b	Block
	Net Expression
	Solder Dot
L	Note–Text
n	Note–Shape

	CHECK
x	Current Cellview
	Hierarchy
	Options
	Rules Setup
	Label Attachment
g	Find Marker
^ g	Delete Marker
	Delete All Markers
	Simulation Monitors

	OPTIONS
O	Editor
o	Display
^ f	Select Filter
	Check
	Check Rules Setup
	Parameter Filter
	Save Defaults
	Load Defaults

Symbol Editor Bindkey Chart

DESIGN

X	Check and Save
S	Save (not needed)
^ s	Save As
E	Hierarchy–Descend Edit
e	Hierarchy–Descend Read
	Hierarchy–Edit In Place
	Hierarchy–Show Scope
^ e	Hierarchy–Return
	Hierarchy–Return To Top
	Create Cellview
	New
	Open
	Discard Edits
	Make Read Only
	Make Editable
9	Probe–Add Net
	Plot

WINDOW

z	Zoom In
]	Zoom In By 2
[	Zoom Out By 2
↓	Pan Down
←	Pan Left
→	Pan Right
↑	Pan Up
f	Fit
F6	Redraw
	Utilities
	Close

EDIT

u	Undo
U	Redo
m	Stretch
c	Copy
M	Move
Del	Delete
r	Rotate
q	Properties–Objects
Q	Properties–Cellviews
	Reset Invisible Labels
^ f	Select–Filter
	Search
	Origin

ADD

p	Pin
	Shape
l	Label
	Selection Box
L	Note ⇒ Text
n	Note ⇒ Shape
	Net Expression
	Custom Pin
	Import Symbol

CHECK

x	Cross View Check
g	Find Marker
^ g	Delete Marker
	Delete All Markers

OPTIONS

O	Editor
o	Display
^ f	Select Filter
	Save Defaults
	Load Defaults

Layout Bindkey Map

F keys						
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**
Help	Save		Toggle Partial Select	Open Design	Maintain Connec-tions	Guided Path
F8	**F9**	**F10**	**F11**	**F12**		
Guided Path Create	Filter Size					

Alphabet keys				
Key to Map: 1=Top row is Control + key 2=Middle row is Shift + key 3=Bottom row is key				
A	**B**	**C**	**D**	**E**
1 Select All	1	1 Interrupt	1 Deselect All	1
2 Select Area	2 Return	2 Chop	2 Deselect Area	2 Display Ops.
3 Select	3 Go to Level	3 Copy	3 Deselect	3 Edit Options

Layout Bindkey Map

F	**G**	**H**	**I**	**J**
1 View 0	1		1	
2 View 32	2 Zoom To Grid		2	
3 Fit All	3 Toggle Gravity		3 Create Instance	
K	**L**	**M**	**N** Snap mode options:	**O**
1	1	1	1 diagonal	1
2 Clear Rulers	2	2 Merge	2 orthogonal	2 Rotate
3 Draw Rulers	3 Label	3 Move	3 L90XFirst	3 Create Contact
P	**Q**	**R**	**S**	**T**
1 Create Pin	1	1 Redraw	1 Split	1 Zoom to Set
2 Create Polygon	2 Design Prop	2 Reshape	2 Search	2 Tree
3 Create Path	3 Object Prop	3 Create Rectangle	3 Stretch	3 Layer Tap
U	**V**	**W**	**X**	**Y**
1	1 Type in CIW	1 Close	1 Fit Edit	1 Cycle Select
2 Redo	2	2 Next View	2 Descend	2 Paste
3 Undo	3 Attach	3 Previous View	3 Edit-In-Place	3 Yank
Z	**Esc**	**Tab**	**Delete**	**Back Space**
1 Zoom In x2	Cancel	Pan	Delete	Undo Point
2 Zoom out x2				
3 Zoom In				
Return Enter last point				

Layout Bindkey Map

Arrow keys				
Control + key: Fit cell to portion of window Shift + key: Move Cursor Key: Pan to portion of cellview				
R7 Home up left	**R8** ↑ top	**R9** PgUp up right		
← **R10** left	**R11** center	**R12** → right		
R13 End down left	**R14** ↓ bottom	**R15** PgDn down right		

Symbol keys on arrow key pad					
= R4	**/ R5**	*** R6**	**-**	**+**	**Enter**
Moves cursor .5 grid points when used with Shift and arrow keys	Moves cursor 1 grid point when used with Shift and arrow keys	Moves cursor 2 grid points when used with Shift and arrow keys	Delete reference point	Set reference point	Enter point

Project I: Simulate Transistor Parameters

- For an npn transistor in PDK lib, analyze, simulate, compare and discuss the following parameters:

(1) 5130/6130: Current gain: $\beta(f), f_T(I_C)$

(2) 6130: Trans-conductance efficiency: $g_m(V_{BE}), \frac{g_m}{I_C}(I_C), C_{jeb}, r_b(L_{emit})$

(3) Bonus: Impedances (real and imaginary parts) looking into the 3 terminals with sweep of frequency and bias current.

(4) Bonus: More simulations and analysis on transistor parameters are encouraged. Simulate MOS parameters.

- Project report due on 10/6, Email your report in yourname_proj1.doc format to daifa01@auburn.edu.

- Carefully document your test procedure including illustration of test benches and steps to plot the parameters. Explain your results with equations and device models. Compare your results with available data given in Model Reference Guide.