RF transistor mini project 1, updated 11/8 class. Save all graphs in a separate folder or paste them in a document.

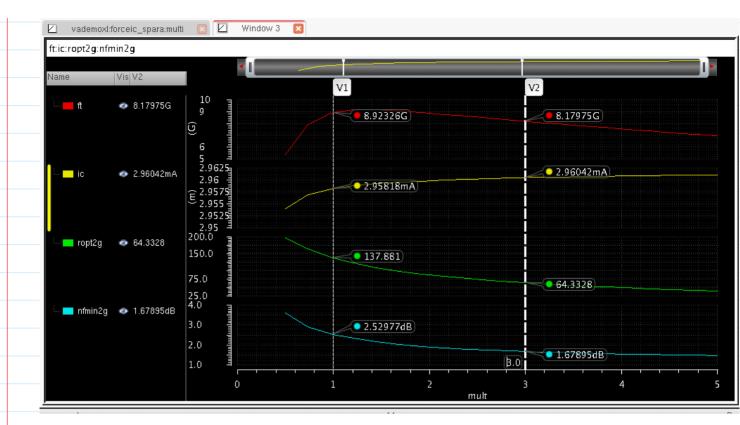
Tuesday, November 06, 2012 6:07 PM

- Using the verilog-a Mextram transistor model, run sparameter simulation to generate the following frequency dependence plots from 10MHz to 10GHz, for VBE=0.5, 0.85 and 0.9V. Set VCE=5.0V. You can do this with calculator or ocean script.
 - a. All of the 4 y-parameters, real and imaginary part, versus frequency. Use a new subwindow for each parameter, i.e. you use 8 subwindows.
 - b. Repeat the above plot with log scale frequency
 - c. Real and imag S11, S21, S12 and S22 versus frequency.
 - d. Repeat the above plot with log scale frequency
 - e. S11 and S22 on Smith chart. S21 and S12 on polar plot. Move cursor and observe how the value of S11 and corresponding r and x values change with frequency.
 - f. Real and imag of zs11 with zs11 defined as the impedance corresponding to a reflection coefficient of S11.
 - g. Mag(h21*frequency) versus frequency
 - h. Real and imag of the Y21/Y11 ratio.
 - i. Real and imag of h21. Compare this with Y21/Y11 ratio.
 - j. Plot out the mag of all s-parameters versus linear frequency on the same plot.
- 2. In "sp" analysis, set frequency to 3GHz. Sweep VBE between 0.75 to 0.9 in 15 steps. VCE=5V. Plot out mag(h21), db20(h21), ft. and mag(s21), db20(s21) as a

function of VBE.

- Place two identical transistors in parallel. Re-run your frequency dependence simulation at the same VBE= 0.85V, VCE=5V. Overlay the Y-parameter plots obtained using a single transistor and 2 transistors. Verify that all of your Y-parameters are exactly doubled.
- 4. Plot out ft-VBE for single transistor and double transistor.
- 5. (newly added 11/8 class) for the same transistor you have been using, create a ADE state that simulates ft calculated from mag(h21)*f at 2GHz versus mult for IC=3mA, VCE=3V. Your multi is a design variable, and should be swept from 0.1 to 5 in 10 steps. Change your "sp" analysis to sweep frequency from 1GHz to 3GHz using 3 steps to keep data file small. Use the technique we described today to hold your current constant as you change size. How much did your ft. change over this large size change?

Below is a sample result of mine, I also checked "noise" in "sp" analysis. Here I plot out minimum noise figure Nfmin at 2GHz, and ft versus mult (size) for a fixed IC. I also showed the actual IC measured at the collector - it is indeed very close to our intended IC, and is practically held constant as mult is swept.



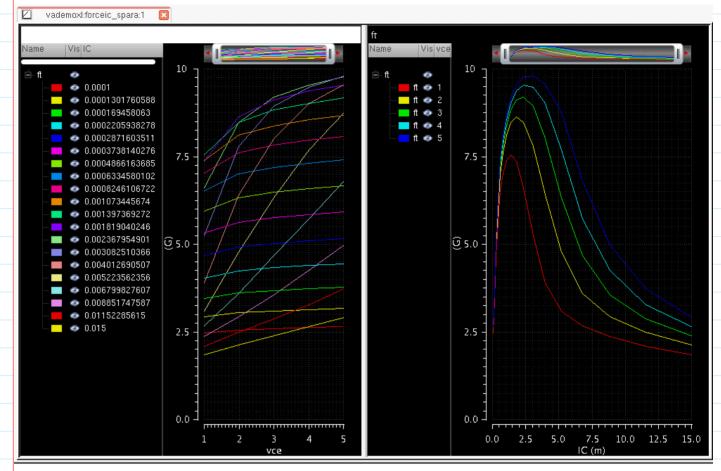
As you increase mult from 1 to 3, ft. decrease from 8.9GHz to 8.2GHz, however, Nfmin decreases from 2.5dB to 1.7dB, a much bigger change.

This type of plot is extremely useful in design of lownoise amplifiers. I also plotted out Ropt - the noise matching source resistance, just ignore that if you have not come across it before in circuit classes.

Required for tcad2 group students, optional for others - this will take a bit more time

- 1. Plot out 1/(2*pi*ft)-1/IC for VCE=5V. Determine the forward transit time tau_f.
- Plot out ft-Ic for single transistor and double transistor.
- 3. (added 11/8) using the new circuit technique, sweep

IC and produce a smooth ft.-IC curve that covers the rise and fall of ft. nicely. Do this for multiple VCE=1, 3 and 5V. Your curves should look like this:



I have given you the LNA schematic. You can modify yours or use this one as is.

Use the same transistor you have been using.

Follow the case study we went over today to design a 2GHz LNA with 3mA current constraint. Set VCE=3V.

I just found out there is no way to construct a complex waveform from two real waveforms in cadence. So you cannot write yopt = gopt + j*bopt.

Cadence gives you gopt and bopt. You need to calculate ropt yourself.

What I did is define an output "bopt" as:

```
getData "/Bopt" ?result "sp_noise" Then "gopt" as:

getData "/Gopt" ?result "sp_noise"
```

From these two, calculate "ropt" which is real part of zopt = 1/yopt = 1/(gopt + jbopt)

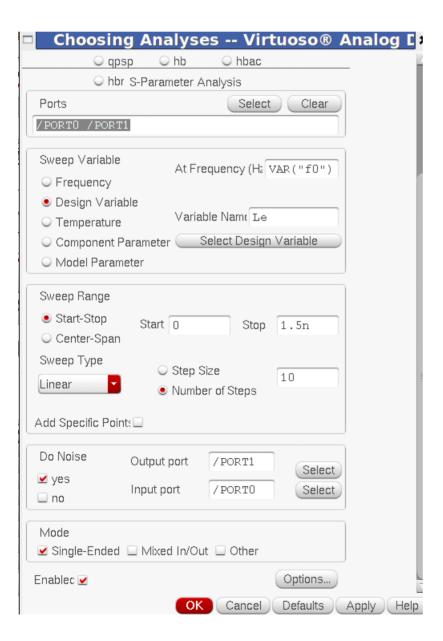
```
[gopt / ((gopt**2) + (bopt**2))]
```

Read today's notes. You will find the 3 steps leading to a good design.

- 1. Sweep "mult" to set ropt=50ohms
- 2. Sweep "Le" to set zs11r = 1 (normalized)
- 3. Sweep "Lb" to set zs11i = 0

Remember to check 'noise' for "sp" analysis.

Below is a screen shot of my "sp" analysis for sweeping "Le":



Go ahead and give this a try. You can in principle turn this into your final project.

Linear 2-port parameters

Saturday, October 27, 2012 9:28 PM

Y

Ζ

Н

ABCD

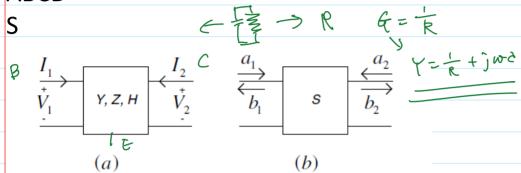


Figure 5.9 (a) Y-, Z- or H-parameters describe the relations among terminal currents and voltages of a linear network. (b) S-parameters describe the relations between the voltage waves, defined as independent linear combinations of terminal currents and voltages.

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}.$$

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}.$$

The Y-parameters can be determined using short-circuit terminations at the input or the output.

$$\begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ V_2 \end{pmatrix}.$$

 H_{11} is essentially the input impedance with the output short circuited ($V_2 = 0$), and H_{21} is the current gain I_2/I_1 with the output short circuited. H_{11} is used to extract the base resistance, and H_{21} is used to extract f_T . Measurement of the H-parameters involves setting I_1 and V_2 to zero.

5.4.4 S-Parameters

At high frequencies, accurate open and short circuits are extremely difficult to achieve because of the inherent parasitic inductances and capacitances. Consequently, the device under test (DUT) often oscillates with open or short terminations. The interconnection between the DUT and test equipment is also comparable to the wave length, requiring the consideration of distributive effects. Because of these practical difficulties, S-parameters were developed and are almost exclusively used to characterize transistor RF and microwave performance.

S-parameters contain no more and no less information than the Z-, Y-, or H-parameters introduced above. The only difference is that the independent and dependent variables are no longer simple voltages and currents. Instead, linear combinations of the simple variables are used to produce four "voltage waves," which contain the same information since they are chosen to be linearly independent. These combinations are chosen such that they can be physically measured at high frequencies using transmission line techniques. One can understand this formulation as a simple transform of the Y-, Z- or H-parameters into a new form,

just like one can transform an impedance
$$Z$$
 to a voltage reflection coefficient Γ

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}.$$
(5.30)

where Z_0 is a characteristic impedance. Such a transform from Z to Γ is extremely useful in studying transmission lines, and the various definitions of two-port parameters provide a similar utility.

The newly defined voltage wave variables a_1 , b_1 , a_2 , and b_2 are shown in Figure 5.9(b), where a indicates incident, and b indicates reflection or scattering. The waves are related to port voltages and currents by

$$a_1 = \frac{V_1 + Z_0 I_1}{2\sqrt{Z_0}}. (5.31)$$

$$b_1 = \frac{V_1 - Z_0 I_1}{2\sqrt{Z_0}}. (5.32)$$

$$a_2 = \frac{V_2 + Z_0 I_2}{2\sqrt{Z_0}}. (5.33)$$

$$a_{1} = \frac{V_{1} + Z_{0}I_{1}}{2\sqrt{Z_{0}}},$$

$$b_{1} = \frac{V_{1} - Z_{0}I_{1}}{2\sqrt{Z_{0}}},$$

$$a_{2} = \frac{V_{2} + Z_{0}I_{2}}{2\sqrt{Z_{0}}},$$

$$b_{2} = \frac{V_{2} - Z_{0}I_{2}}{2\sqrt{Z_{0}}}.$$
(5.31)
$$(5.32)$$

$$(5.33)$$

The voltage waves are defined using voltages and currents for a characteristic impedance Z_0 , similar to the definition of Γ in transmission lines. These voltage waves are not "voltages" per se, but voltages normalized to a $2\sqrt{Z_0}$ term such that when squared they have dimensions of power. The voltages a_1 and a_2 are called the incident waves, and b_1 and b_2 are called the scattered waves. The scattered waves are related to the incident waves by a set of linear equations, just as the port voltages are related to the port currents by the Z-parameters

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}. \tag{5.35}$$

The coefficients of these relationships are the S-parameters. One can mathematically prove that the resulting S-parameters are unique for a given linear network, just as they are for the Z-, Y-, and H-parameters.

The measurement of S-parameters involves setting a_1 and a_2 to zero, which is easily accomplished by terminating the ports with Z_0 . For instance, to set $a_2 = 0$, we terminate port 2 with Z_0 . As a result, $v_2 = -I_2Z_0$, and thus $a_2 = 0$ according to the definition of a_2 . Using the definitions of a_1 and b_1 , S_{11} is then obtained as

$$S_{11} = \frac{b_1}{a_1} = \frac{V_1 - I_1 Z_0}{V_1 + I_1 Z_0} = \frac{Z_{in,0} - Z_0}{Z_{in,0} + Z_0}.$$
 (5.36)

where $Z_{in,0} = V_1/I_1$ is the input impedance with $Z_1 = Z_0$. We see then that S_{11} is therefore simply the reflection coefficient corresponding to the input impedance when the output is terminated with Z_0 . The required condition for S-parameter measurements is hence termination with the proper characteristic impedance, just as for short-circuit termination for Y-parameters, or open-circuit termination for Z-parameters. Similarly,

$$S_{21} = \frac{b_2}{a_1} = \frac{V_2 - I_2 Z_0}{V_1 + I_1 Z_0} = 2 \frac{V_2}{V_1 + I_1 Z_0} = 2 \frac{V_2}{V_s}.$$
 (5.37)

where $V_s = V_1 + I_1 Z_0$ is equal to the source voltage if a source impedance Z_s is chosen to be Z_0 , as illustrated in Figure 5.10. We note that $Z_s = Z_0$ is indeed used in practical S-parameter measurements. We see that S_{21} is simply twice the ratio of V_{out} to V_s for a Z_0 source and a Z_0 load. This relationship provides a simple means of calculating S_{21} and S_{11} using the transistor equivalent circuit, and understanding the physical meanings of S_{21} and S_{11} in terms of impedance and voltage gain, which are familiar to analog designers. Another physical meaning of S_{21} is that $|S_{21}|^2$ gives the transducer gain for a Z_0 source and Z_0 load.

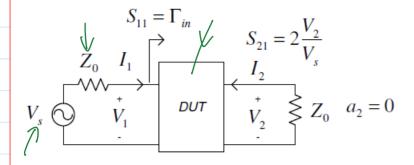


Figure 5.10 A simple method of calculating S_{11} and S_{21} . With a Z_0 drive and a Z_0 load, S_{11} is the input reflection coefficient looking into port 1, and S_{21} is twice the voltage gain V_2/V_s .

The measurements of S_{22} and S_{12} are similar. We terminate port 1 with a Z_0 load, and drive port 2 with a Z_0 source. S_{22} is essentially the output reflection coefficient looking back into the output port for a Z_0 source termination, S_{12} is the reverse gain, and $|S_{12}|^2$ is the reverse transducer gain for a Z_0 source and a Z_0 load.

Because of their intuitive relationship to the reflection coefficients, S_{11} and S_{22} are conveniently displayed on a Smith chart, while S_{21} and S_{12} are typically displayed on a polar plot. Figure 5.11(a) and (b) show an example of the S_{11} and S_{21} measured from 4 to 40 GHz for a SiGe HBT. Two collector currents of 1.26 mA and 25.0 mA are shown, with $V_{CB} = 1$ V. We see that the S_{11} for a bipolar transistor always moves clockwise as frequency increases on the Smith chart. The S_{11} data at higher I_C in general shows a smaller negative reactance, because of the higher EB diffusion capacitance. The S_{21} magnitude decreases with increasing frequency, as expected, because of decreasing forward transducer gain, while S_{21} is larger at higher I_C because of the higher I_T at that bias current. It follows from the above discussions that the S-parameters of a SiGe HBT will intimately depend on the transistor size, biasing condition, and operating frequency.

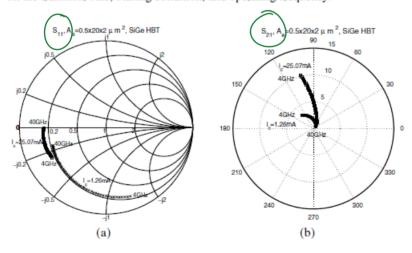
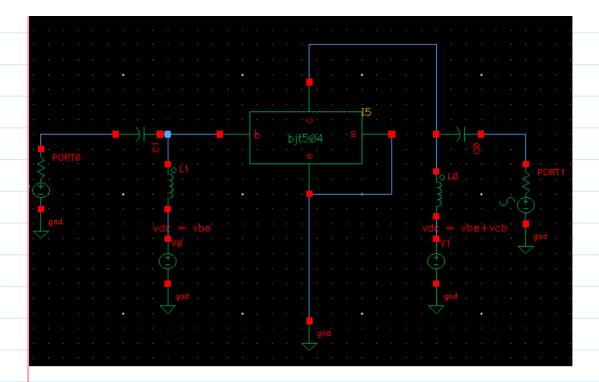


Figure 5.11 Example plots of (a) S_{11} and (b) S_{21} measured data for a SiGe HBT. Two traces are for $I_C=1.26$ and 25 mA, with $V_{CB}=1$ V. The frequency range is from 4 to 40 GHz, and $A_E=0.5\times 20\times 2\mu \mathrm{m}^2$.

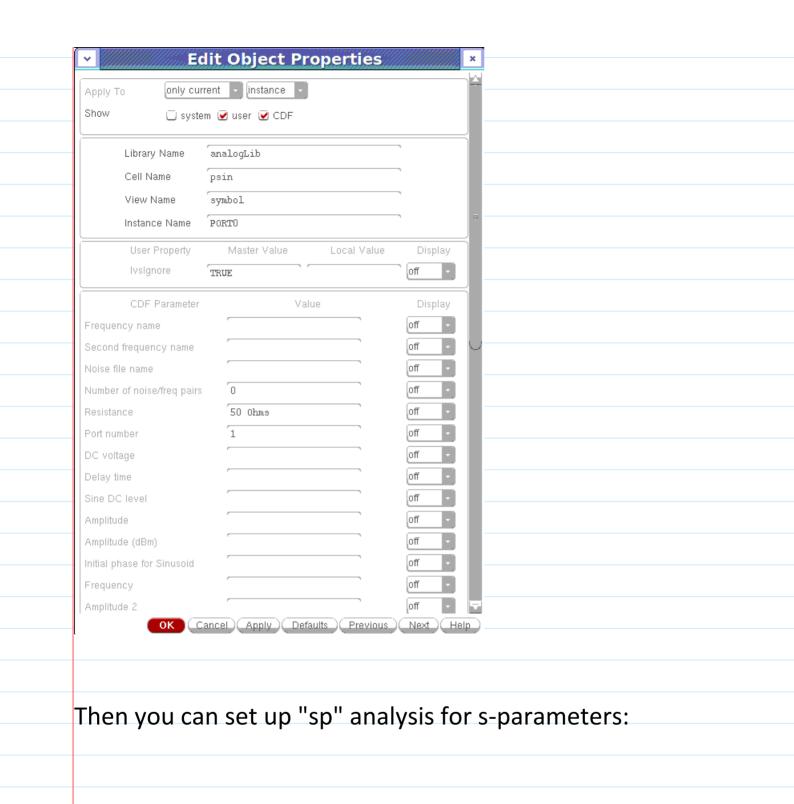
$$\frac{z}{z} = r + jx$$

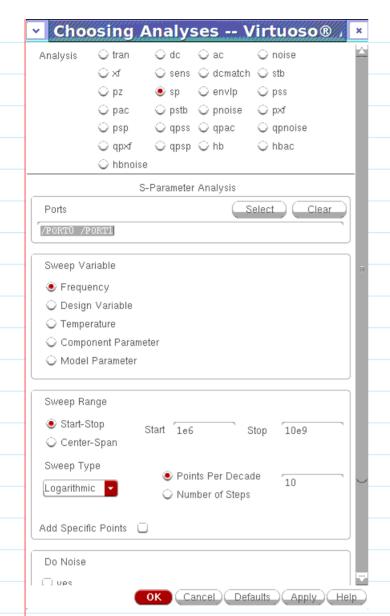
s-parameter simulation and measurement Tuesday, October 30, 2012 9:38 AM We need to combine dc bias with RF excitation using bias tees - essentially an inductor that passes DC and blocks ac (RF), and a capacitor that passes RF and blocks dc. Copy the vademo folder from /scratch/8710/cadence To your own \$HOME/cadence folder or another folder (if so, modify the cds.lib after copying) Open terminal Then go to (cd) that folder of yours, type "source cadence6" Then type "virtuoso" on command line.



Pay attention to the "PORTO" and "PORT1" - they are from the analogLib, under sources.

Specify the port number as "1" and "2" for the input and output ports. An example is shown below:





You can type in or select from schematic the ports, for most part, we specify two ports.

A frequency sweep is basic, of course, you can sweep other parameters like you did before.

Plotting and understanding transistor s-parameters

Thursday, November 01, 2012 9:46 AM

You can of course use the GUI to manually do plotting. Problem is that Cadence does not have a nice way of keeping all of your plot settings so you can reuse them when you run a new simulation.

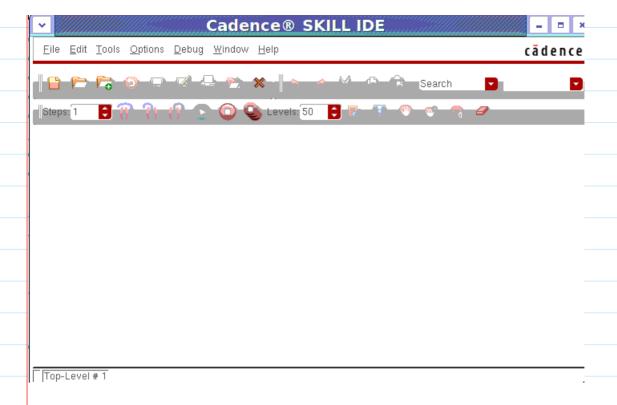
Other tools like Agilent does better in this regard.

However, verilog-a support is much better in cadence, also many design kits support cadence (there is ADS link too but that requires additional kit support you often do not have)

Cadence has scripting, so you can use ocean - but it is difficult for the average user, they are designers not programmers.

I experimented with it and came up with a piece of ocean program for teaching - you should find this useful for research too.

From the menu of the very first "virtuoso" window, "Tools-Skill IDE"



Then "File -> Open" to open the only plotbjtspara.ocn in the folder that you copied from me.

I wrote it so it will work with both cadence ic5 and ic6. Also I wrote it in a way that allows you to copy these expressions into your "Outputs" or "calculators" - so some expression options may seem unnecessary if you just use it for ocean.

You will see that I made conversion between reflection coefficient and impedance in two occasions.

- S11 I created "zs11" which is the normalized impedance for a Gamma = S11. I plot out S11 on "Smith" chart, and then plot out real and imag of zs11.
 - a. Look at both plots together, use cursor to move

- along data on Smith chart, observe the "r+jx" number the program reports.
- b. Compare that with what is on the real(zs11) and imag(zs11) vs freq curves. You will find they are consistent
- 2. H11 h11 is the input impedance for an output short circuit termination. So I convert H11 to a reflection coefficient "gh11" so that you can then plot it on Smith chart.
 - a. Move cursor along data on smith watch the "r+jx" output, compare that with your own plotting of real and imag of h11, well you can normalize to z0 easily for exact apple-to-apple comparison
- 3. Try to compare S11 and H11.

Current gain with output shorted and fT

Saturday, October 27, 2012 9:37 PM

5.3.1 **Current Gain and Cutoff Frequency**

The high-frequency current amplification capability of a SiGe HBT is typically measured by the small-signal current gain for a shorted output termination (i.e., h_{21}). Imagine driving the base terminal with a small-signal current $i_b = i_0 e^{j\omega t}$, and now short-circuit the output (collector), as shown in Figure 5.3. The node voltage vb then equals

$$v_b = \frac{1}{g_{be} + j\omega(C_{be} + C_{bc})} i_b.$$
 (5.4)

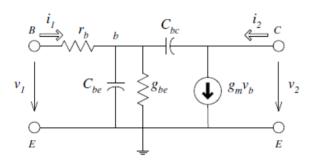


Figure 5.2 A simple high-frequency equivalent circuit model.

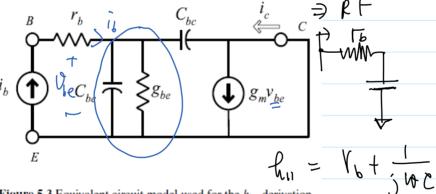


Figure 5.3 Equivalent circuit model used for the h_{21} derivation.

The effective capacitive load for the input due to Miller capacitance C_{bc} is still C_{bc} because of the "zero" voltage gain resulting from the short-circuited output. Because the reverse-biased CB junction capacitance is far smaller than the forwardbiased EB junction capacitance, we can neglect its contribution to the output current ic

$$i_c \approx g_m v_b = g_m g_{be} + j\omega(C_{be} + C_{bc}) i_b.$$
 (5.5)

Therefore, we have

$$i_{c} \approx g_{m}v_{b} = \underbrace{\frac{g_{m}}{g_{be} + j\omega(C_{be} + C_{bc})}} i_{b}.$$
(5.5)

efore, we have
$$h_{21} = \frac{i_{c}}{i_{b}} \Big|_{v_{c}=0} = \underbrace{\frac{g_{m}}{g_{be} + j\omega(C_{be} + C_{bc})}} = \frac{\beta}{1 + j\omega(C_{be} + C_{bc})/g_{be}}.$$
(5.6)

Note that h_{21} is constant at low frequencies, and then decreases at higher frequencies. Obviously, the imaginary part increases with ω , and dominates at high frecies. Obviously, the imaginary part increases with ω , and dominates at high fre-

quencies. Under these conditions the above equation becomes

$$h_{21} = \frac{g_m}{j\omega(C_{be} + C_{bc})}.$$

 $\lim_{m \to \infty} w = w_{\tau} = \frac{g_m}{C_{\text{get}}(g_m)}$

which is equivalent to

$$h_{21} \times f = \frac{f_T}{j}.$$

$$f_T = \frac{g_m}{2\pi (C_{be} + C_{bc})}.$$
(5.8)

The $|h_{21} \times f|$ product is a constant over the frequency range where these assumptions hold. This constant is referred to as f_T , the transition frequency, or more commonly, the cutoff frequency. In practice, f_T is extracted by extrapolating the measured $|h_{21}|$ versus frequency data in a range where a slope of -20 dB/decade is observed. The frequency at which the extrapolated $|h_{21}|$ reduces to unity is defined to be f_T (i.e., the unity gain cutoff frequency). Practically speaking, the extrapolation is necessary here because we are usually not interested in operating transistors at the frequency of unity current gain, which can be different from the extrapolated f_T , depending on parasitics and other factors. Instead, we are interested in the gain available at much lower frequencies where the current gain is much higher than unity. In the frequency range where $|h_{21}|$ rolls off at -20 dB/decade, $|h_{21}|$ can be easily estimated as f_T/f .

State-of-the-art SiGe HBTs exhibit f_T values above 200 GHz [1], which is much higher than the operating frequencies of the bulk of existing wireless systems, which are typically below 10 GHz. In this case, caution must be exercised in estimating $|h_{21}|$ from f_T , because the operating frequency f may be below the frequency range over which $|h_{21} \times f| = f_T$. In this case, we then need to resort to (5.6) which applies to all frequencies below f_T and can be rewritten as follows using (5.9)

$$h_{21} = \frac{\beta}{1 + jf/f_{\beta}}.$$

$$f_{\beta} = \frac{f_T}{\beta}.$$
(5.10)

Here, $|h_{21}|$ is equal to β at low frequencies, reduces by 3 dB at $f = f_{\beta} = f_T/\beta$, and then drops off with increasing f at a theoretical slope of -20 dB/decade. Hence, for

 $^{^{1}}$ We note that for the very high f_{T} SiGe HBTs being realized today (200+ GHz), instrumentation limitations place a practical upper bound on directly measuring f_{T} in any case, since the highest reliable measurement frequencies are in the 110-GHz range for commercially available test systems.

a SiGe HBT with $f_T = 100$ GHz and $\beta = 100$, the 3 dB frequency is $f_\beta = 1$ GHz. For a design frequency of 2 GHz, which is close to f_β , (5.11) needs to be used for $|h_{21}|$ estimation instead of f_T/f . Figure 5.4 shows an example of measured h_{21} versus frequency from 2 to 110 GHz for a SiGe HBT. The extrapolated f_T is 117 GHz. A noticeable deviation from the 20-dB/decade straight line fit is observed below 7 GHz, necessitating the use of (5.11) for h_{21} estimation. Note as well that a deviation from the 20-dB/decade slope is observed above 40 GHz.

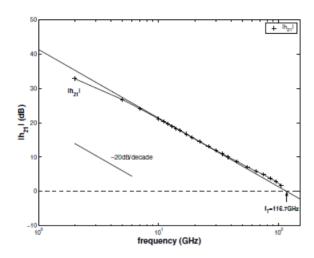
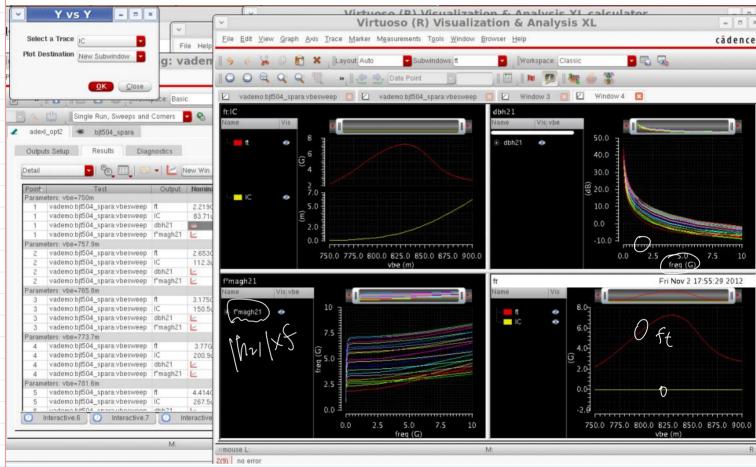


Figure 5.4 Measured $|h_{21}|$ versus frequency for a state-of-the-art SiGe HBT.

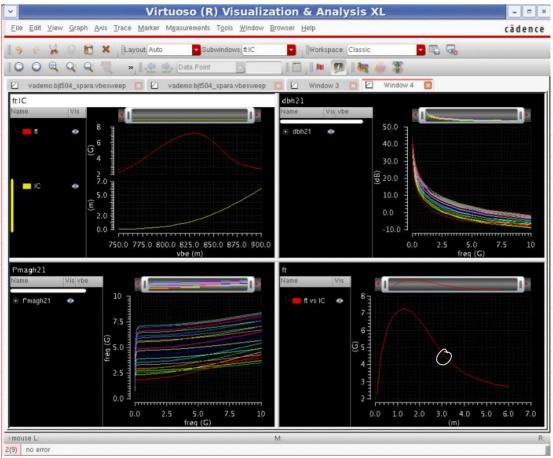
Look for a region where magh21 (mag of h21) * freq is frequency independent

Choose a freq point from this region, the magh21 * freq product is ft.

use "Y vs Y" from menu to make ft-IC plot rather than ft-vbe plot:

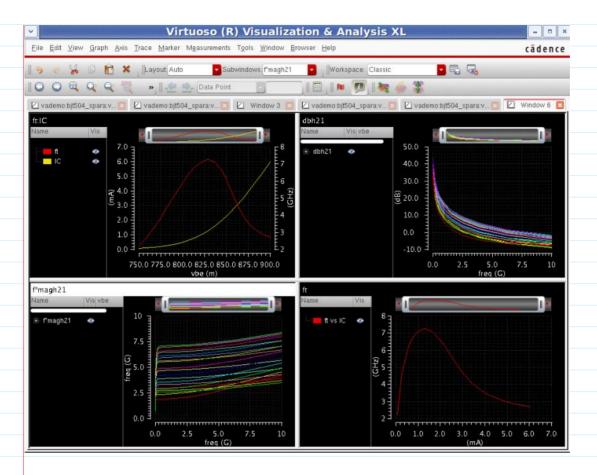


We then have ft-Ic plot:

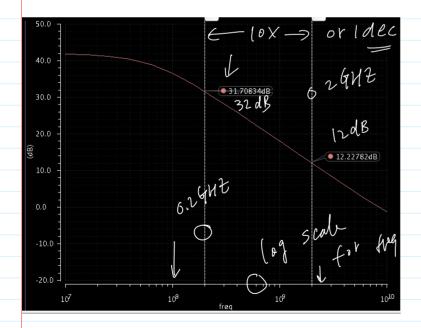


With a bit extra work in the "Outputs setup", we can add units and suffix to our like, e.g. using GHz for ft. and using mA for IC

This gives us a nice summary of our h21 and ft. data:



You can also inspect db20(h21) vs log scale freq, and identify the 20dB/decade slope:



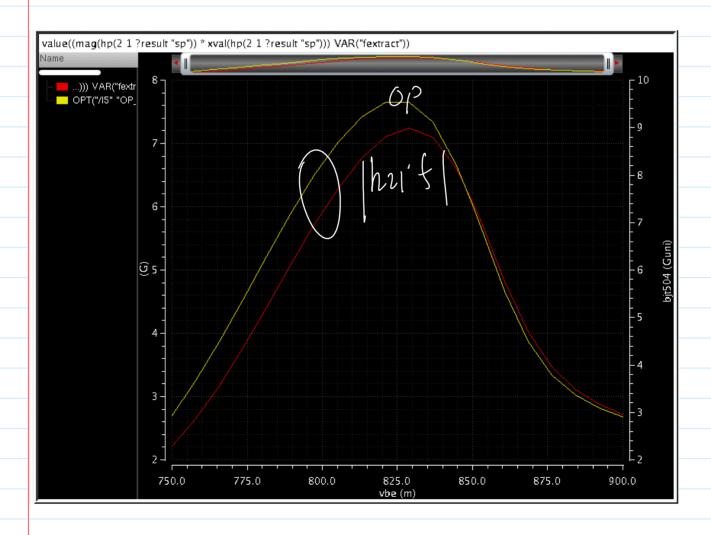
Ft from h21 and ft from OP point (approximate)

Saturday, November 03, 2012 3:20 PM

We can compare the ft. obtained from h21 (sp analysis) with the ft. obtained from dc operational point analysis (remember we did that first?)

They are not exactly the same but close.

Also the way we determine ft. should be changed "improved" to make a more fair comparison with the ft. from OP.



Ft and current density

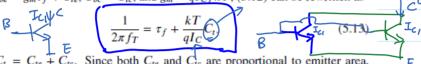
Saturday, October 27, 2012 9:40 PM

5.3.2 Current Density Versus Speed

The fundamental nature of SiGe HBTs require the use of high operating current density in order to achieve high speed. The operating current density dependence of f_T is best illustrated by examining the inverse of f_T using (5.9)

$$\frac{1}{2\pi f_T} = \frac{C_{be} + C_{bc}}{g_m}. (5.12)$$

Since $C_{be} = g_m \tau_f + C_{te}$, $C_{bc} = C_{tc}$, and $g_m = qI_C/kT$, (5.12) can be rewritten as

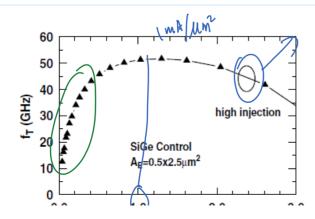


where $C_t = C_{te} + C_{tc}$. Since both C_{te} and C_{tc} are proportional to emitter area, (5.13) can be rewritten in terms of the biasing current density J_C as

where $C'_t = C_t/A_E$ is the total EB and CB depletion capacitances per unit emitter area, and $J_C = I_C/A_E$ is the collector operating current density. Thus, the cutoff frequency f_T is fundamentally determined by the biasing current density J_C , independent of the transistor emitter length. For very low J_C , the second term is very large, and f_T is very low regardless of the forward transit time τ_f . With increasing J_C , the second term decreases, and eventually becomes smaller than τ_f . At high J_C , however, base push-out (Kirk effect, refer to Chapter 6) occurs, and τ_f itself increases with J_C , leading to f_T roll-off. A typical f_T versus J_C characteristic is shown in Figure 5.5 for a first generation SiGe HBT.

The values of τ_f and C_t' can be easily extracted from a plot of $1/2\pi f_T$ versus $1/J_C$, as shown in Figure 5.6. Near the peak f_T , the $1/2\pi f_T$ versus $1/J_C$ curve is nearly linear, indicating that C_t' is close to constant for this biasing range at high f_T . Thus, C_t' can be obtained from the slope, while τ_f can be determined from the y-axis intercept at infinite current $(1/J_C = 0)$.

To improve f_T in a SiGe HBT, the transit time τ_f must be decreased by using a combination of vertical profile scaling as well as Ge grading across the base. At the same time, the operating current density J_C must be increased in proportion in order to make the second term in (5.14) negligible compared to the first term (τ_f). That is, the high f_T potential of small τ_f transistors can only be realized by using sufficiently high operating current density. This is a fundamental criterion for high-speed SiGe HBT design. The higher the peak f_T , the higher the required operating J_C . For instance, the minimum required operating current density has increased from 1.0 mA/ μ m² for a first generation SiGe HBT with 50-GHz peak f_T to 8–10



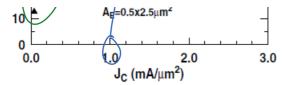


Figure 5.5 A typical $f_T - J_C$ behavior for a SiGe HBT.

mA/ μ m² for >200-GHz peak f_T third generation SiGe HBTs [1]. Higher current density operation naturally leads to more severe self-heating effects, which must be appropriately dealt with in compact modeling and circuit design [2]. Electromigration and other reliability constraints associated with very high J_C operation have also produced an increasing need for copper metalization schemes.

In order to maintain proper transistor action under high J_C conditions, the collector doping must be increased in order to delay the onset of high injection effects. This requisite doping increase obviously reduces the breakdown voltage. At a fundamental level, trade-offs between breakdown voltage and speed are thus inevitable for all bipolar transistors (Si, SiGe, or III-V). Since the collector doping in SiGe HBT is typically realized by self-aligned collector implantation (as opposed to during epi growth in III-V), devices with multiple breakdown voltages (and hence multiple f_T) can be trivially obtained in the same fabrication sequence, giving circuit designers added flexibility.

Another closely related manifestation of (5.14) is that the minimum required J_C to realize the full potential of a small τ_f transistor depends on C'_t . Both C'_{te} and C'_{tc} thus must be minimized in the device and are usually addressed via a combination of structural design, ground-rule shrink, and doping profile tailoring via selective collector implantation. This reduction of C'_{tc} is also important for increasing the power gain (i.e., maximum oscillation frequency $-f_{max}$).

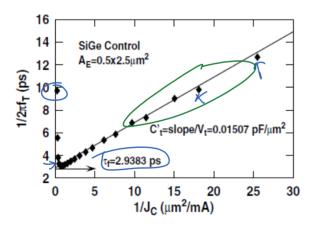
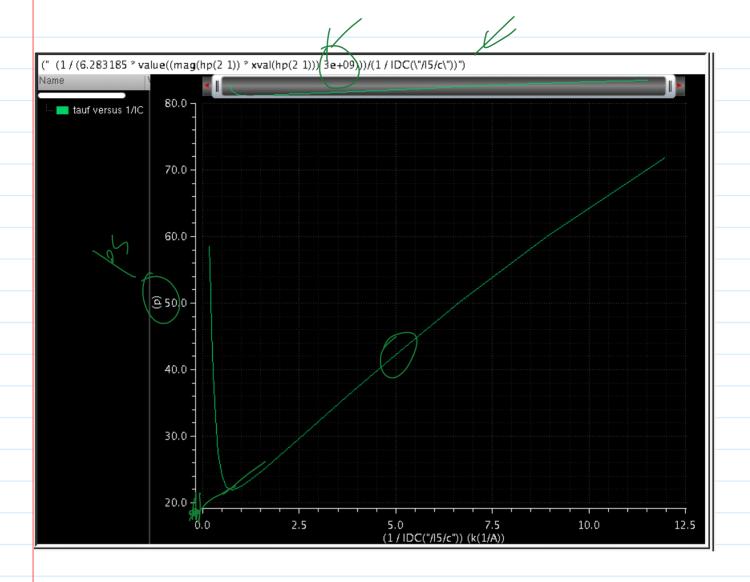


Figure 5.6 Illustration of C'_t and τ_f extraction in a SiGe HBT.

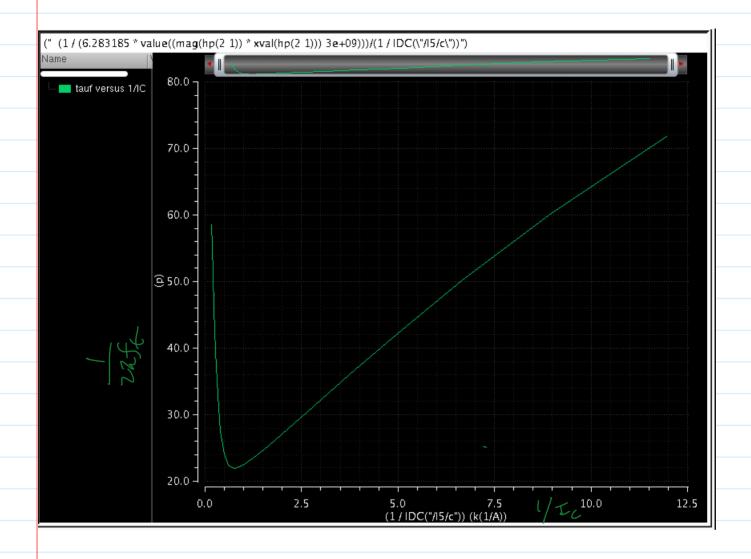
1/(2pi*ft) - 1/Ic

Saturday, November 03, 2012 3:23 PM



Tauf versus phi_t/IC

Saturday, November 03, 2012 3:25 PM



Base resistance extraction using h11 semi circles

Saturday, October 27, 2012 9:41 PM

5.3.3 Base Resistance

Observe that the base resistance r_b does not directly enter the h_{21} expressions, simply because r_b is in series with the ideal transistor (without r_b). In practice, however, r_b limits transistor power gain and noise performance, because it consumes input power and produces thermal noise directly at the base terminal, the worst possible place for the location of a noise source! As a result, minimization of the various components of the base resistance is a major challenge in SiGe HBT structural design, fabrication, and process integration. The base resistance is a key parameter for both process control and circuit design, and deserves careful attention. Unlike many bipolar parameters, base resistance is particularly challenging (and time consuming) to extract in a robust manner.

A popular technique to extract r_b is to use the input impedance with a shorted output, which by definition is equal to h_{11} . An inspection of Figure 5.3 shows

$$h_{11} = Z_{in}|_{v_c=0} = r_b + \frac{1}{g_{be} + j\omega C_i}.$$
 $C_i = C_{be} + C_{bc}.$
(5.15)

The real and imaginary parts of h_{11} are

$$x = \Re(h_{11}) = r_b + \frac{g_{be}}{g_{be}^2 + (\omega C_i)^2}$$

$$y = \Im(h_{11}) = -\frac{\omega C_i}{g_{be}^2 + (\omega C_i)^2}.$$
(5.16)

Using (5.16), one can easily prove that the (x, y) ordered pairs at different frequencies form a semicircle on the complex impedance plane

$$(x - x_0)^2 + y^2 = r^2$$
, (5.17)
 $x_0 = r_b + 1/2g_{be}$ $r = 1/2g_{be}$.

The (x, y) impedance point moves clockwise with increasing frequency. The base resistance is then determined to be the high frequency intercept between the fitted impedance semicircle and the real axis, which appears on the left. This is the socalled "circle impedance" base resistance extraction method. In the above analysis, the emitter resistance r_e is neglected for simplicity, but it can be shown that the extracted r_b is actually the sum of the transistor r_b and r_e . Figure 5.7 shows an example of such an r_b extraction for a typical first generation SiGe HBT with an effective emitter area of $0.5 \times 40 \ \mu m^2$. The h_{11} data was measured from 0.5 to 15 GHz in order to make a meaningful fit to a semicircle. Choosing a proper measurement frequency range is important in reliable r_b extraction, as can be seen from Figure 5.7. In this case, had we used a frequency range of 15-50 GHz, the data would have formed only a tiny portion of the semicircle, making fitting and r_b extraction much more difficult. Deviation from circular behavior is often observed at frequencies close to f_T , and those data should be discarded in the r_b extraction. Given the I_C dependence of f_T , the frequency range over which r_b extraction is made can be varied with I_C to order to obtain an accurate I_C dependence of r_b , which is needed in compact modeling.

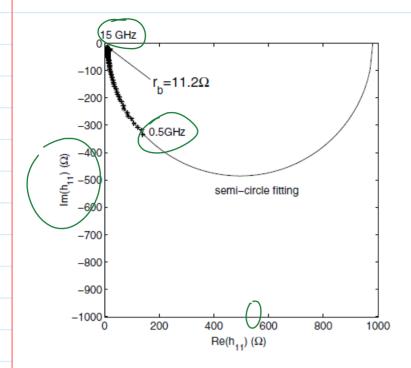
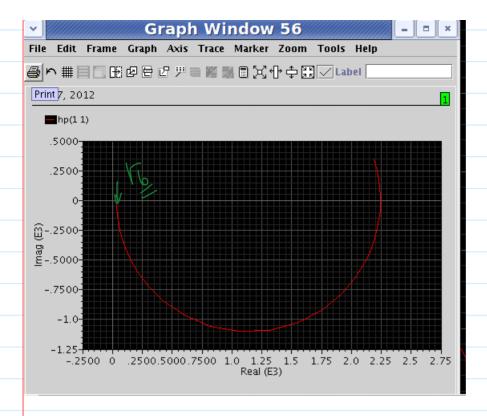


Figure 5.7 Extraction of r_b using the circle impedance method. The measured h_{11} data forms a semicircle. The frequency increases clockwise.

Example:

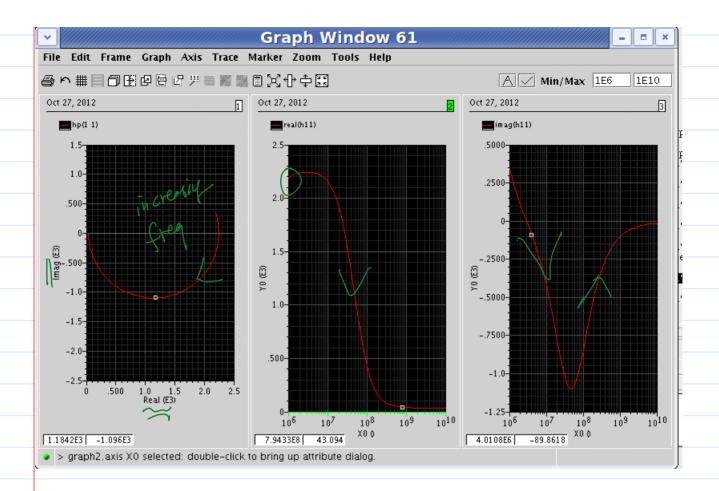
Simulate the h11 behavior for currents around peak ft. of the bjt504 device you have been using.

Plot out Imag-Real h11 as shown below.



Of course with all the parasitics, the simulated h11 does not precisely follow our first order derivation, but it shows the overall behavior nicely. It is indeed close to a semi circle.

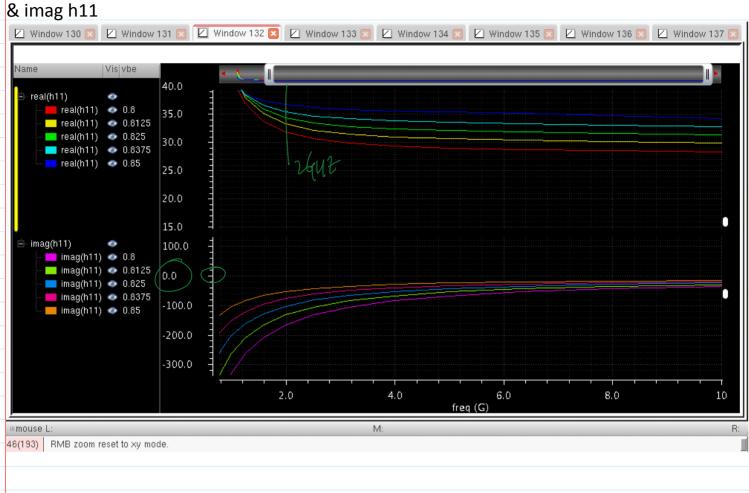
In this simulation, frequency is from 1MHz to 10GHz.



In measurement, it is typical to go from 2GHz to 10GHz (or 26GHz, 40GHz).

Can you explain why at seveal GHz, real(h11) is nearly a constant, while imag(h11) is very small?

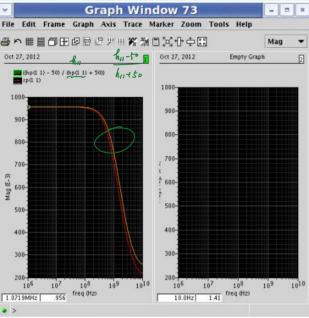
The real part of zs11 first. Now we add more VBE's. Zoom in plots to show higher freq behavior of real & imag h11



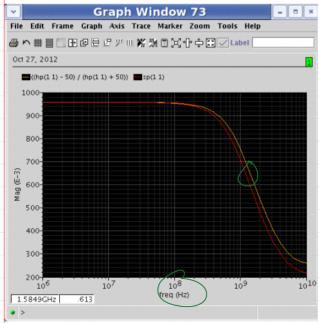
H11 and s11 comparison

Saturday, October 27, 2012 10:28 PM

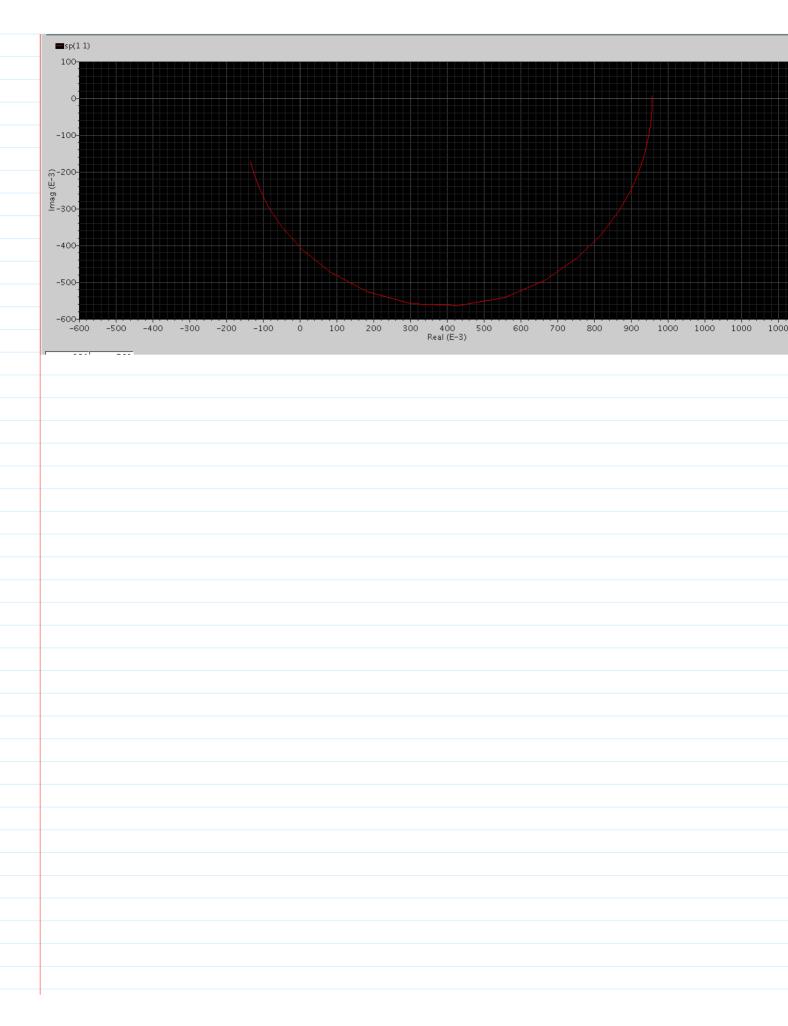
Let us compare s11 and h11 by converting h11 to a reflection coefficient



Some papers use s11 instead of using h11 to extract rb - this can cause some errors.



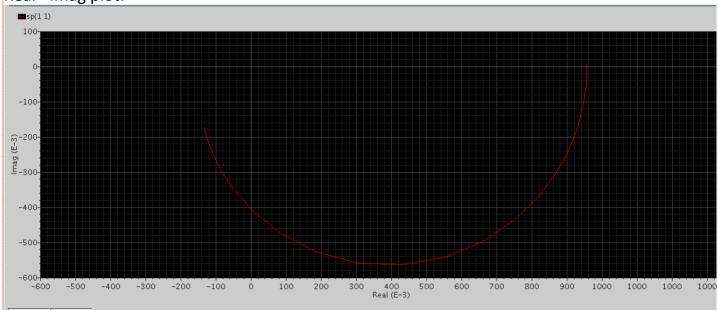
S11, real-imag plot:

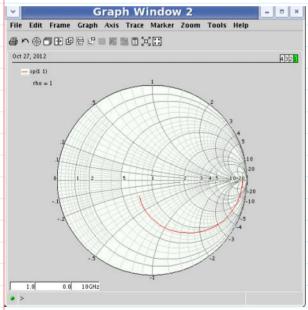


S11 behavior - this also helps you understand smith chart

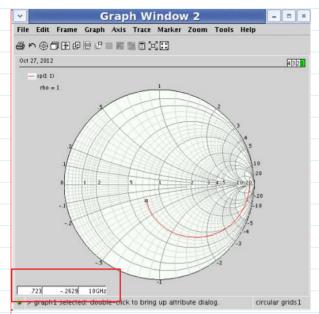
Saturday, October 27, 2012 11:08 PM

Real - Imag plot:



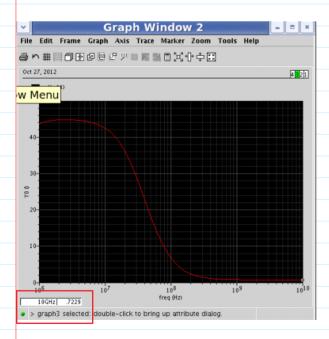


At 10GHz:

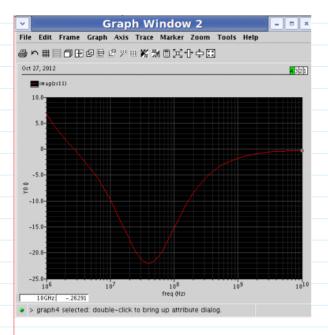


Note: r=0.723, x=-0.2629

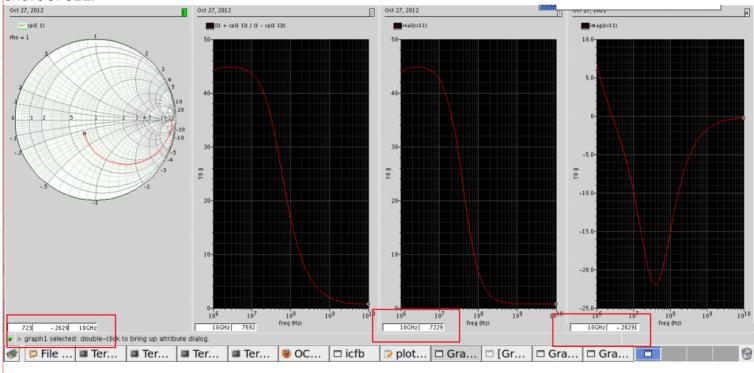
We can calculate zs11 by converting s11 to normalized impedance, zs11 = (1+s11)/(1-s11), then looking at real and imaginary part. Let us look at the real part of zs11 first. I have set cursor to 10GHz, see lower left corner:

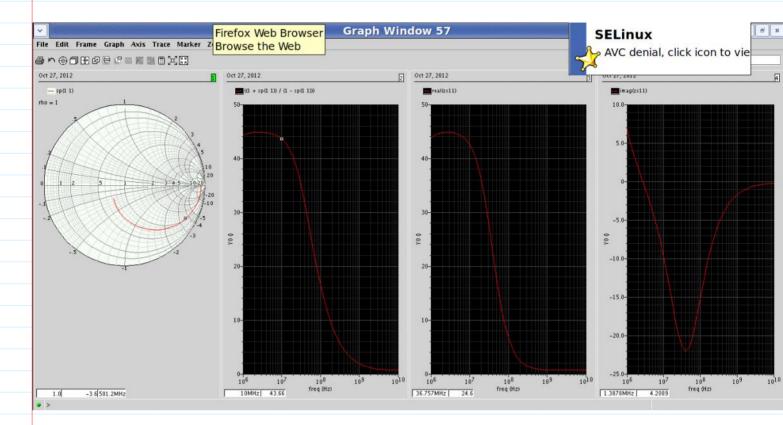


Now the imaginary part, again, note the lower left corner display of imag(zs11):



This is indeed what is displayed as "x" value when we view smith chart of s11.



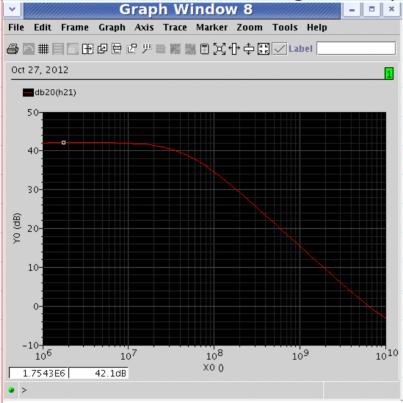


Move cursor and demonstrate the meaning of s11 on smith chart using zs11 = (1+s11)/(1-s11)

Explain why above 2GHz, real part of zs11 - essentially the "r" value of s11 on smith chart is nearly constant in transistors.

Use db20() function.

Also often it is best to use "log" for freq axis.



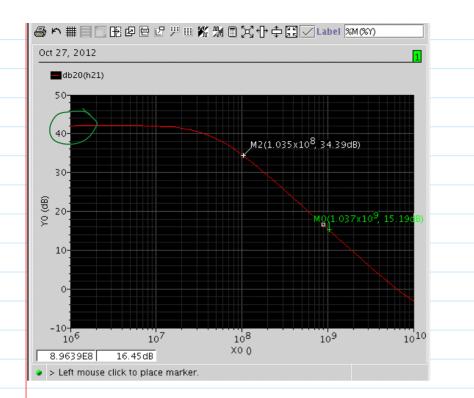
Low-frequency, h21 is flat.

High-frequency, it drops.

The slope is -20dB per decade increase of frequency.

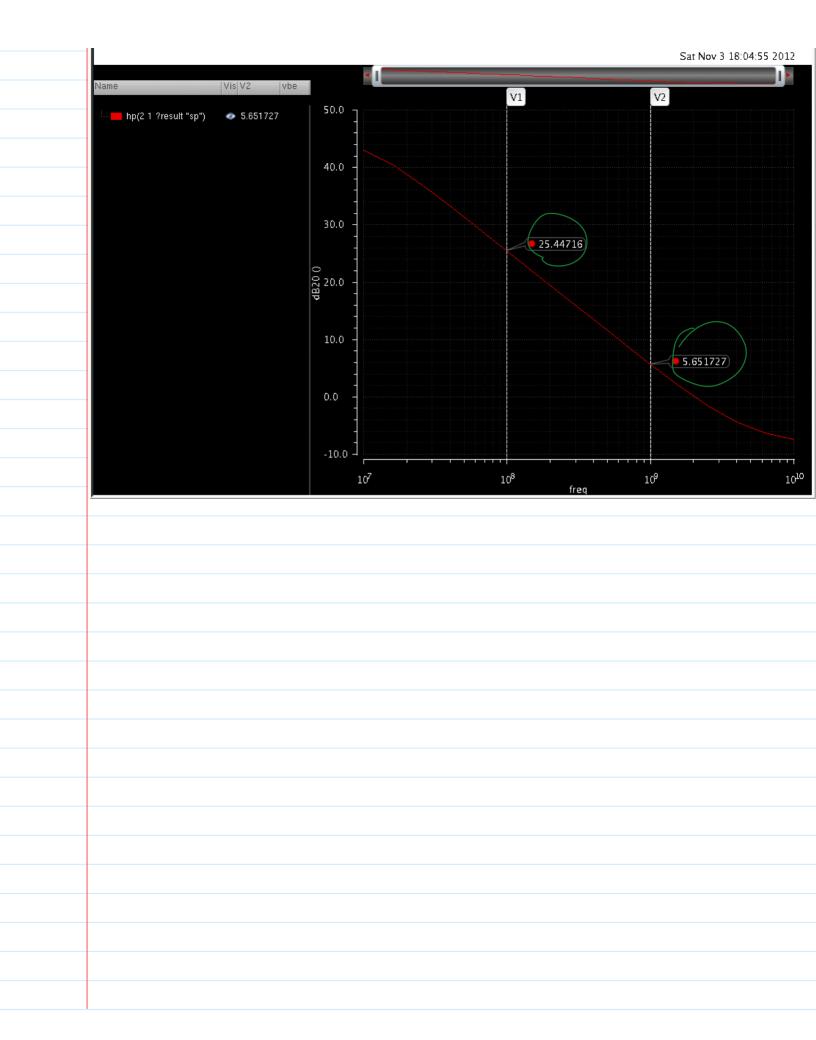
In this region, h21 * f = constant, or ft.





 $h_{21}|_{lorf} \rightarrow B$ $2|_{lod} or$ more

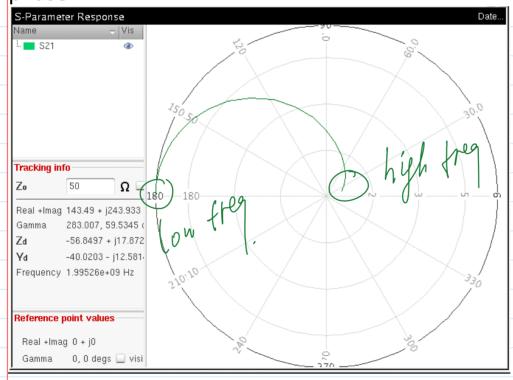
In IC615, see the marker I made at 100MHz and 1GHz, and observe how the y-value differs by about 20dB for 1 decade increase in frequency



Recall that s21 itself is a voltage gain, so db20 is power gain - more accurately, power delivered to a z0 load divided by power available from a z0 source.

Polar showing magnitude and phase:

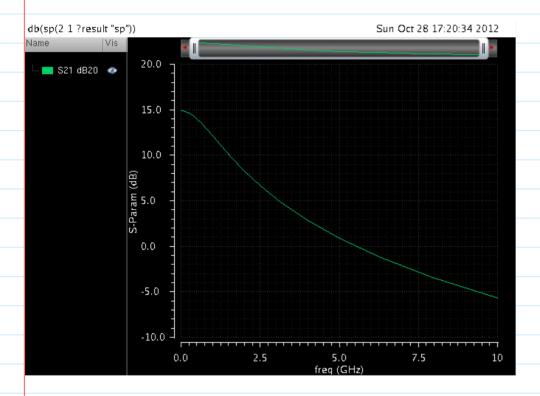
It is typical to plot the original s21 number (without taking db) on polar plot that shows magnitude and phase:



Note that at very low frequency, the phase is 180 degrees, as the amplifier is inverting (180 degree phase diff)

Db20

Use db20(s21) to show its db value.
To just show the magnitude, we can take db20, and use log scale for frequency axis:



Db20 with log freq axis

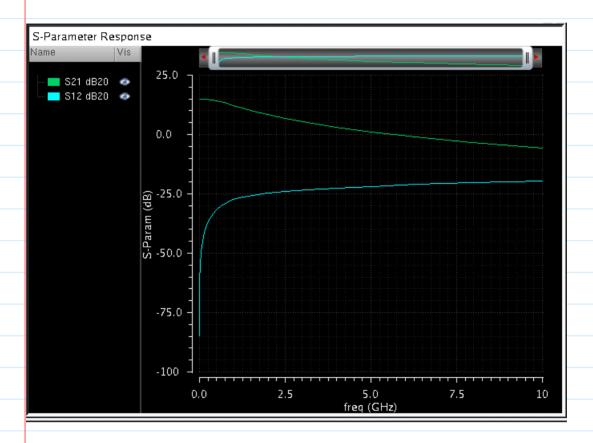


Like h21, there is 20db/decade slope at high frequency.

Comparing h21 and s21 Tuesday, November 06, 2012 10:24 AM					

S12 is reverse transmission coefficient - for transistors in forward mode, this should be small.

To show this we plot out s21 and s12 in db20 together:



Transistor s-parameter analytical calculation and intuitive understanding

Sunday, November 04, 2012 2:31 PM

Consider bipdar transistor (Mos is simpler)

B 16 Cbic TC Color

Reconstitution

E 2 The Color

The

 $i_c + i_1 = g_m o \Rightarrow i_c = g_m o - i_1$

Typically TI << gmd, iz ~ gmd.

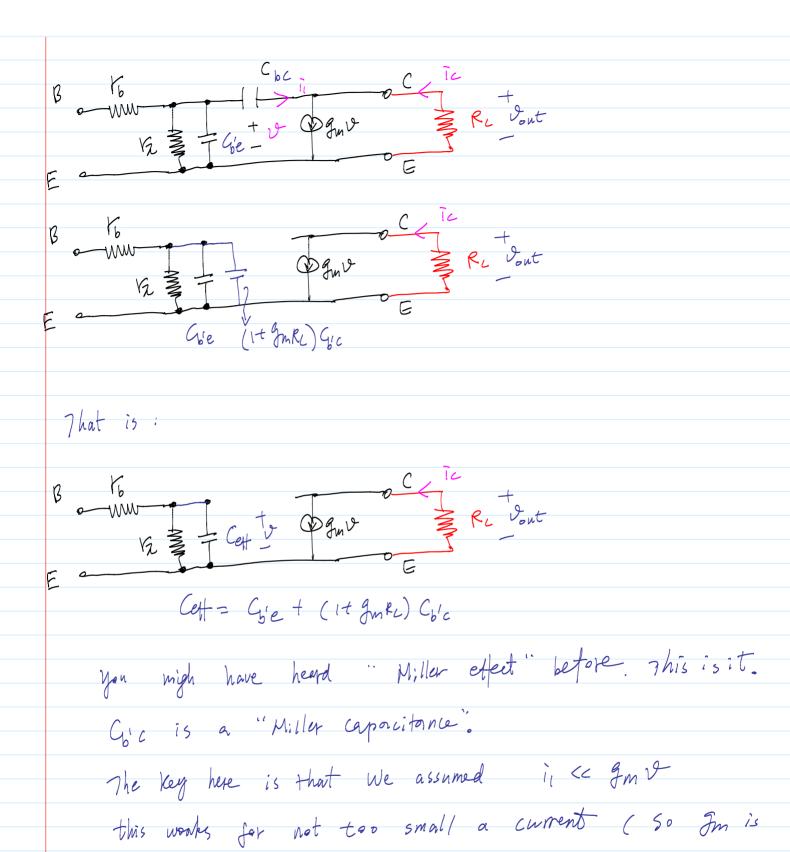
Vout = -ic RL = - 3m RLD -

The current thru Gic is $i_1 = j_{bc} \mathcal{C}_{bc} \mathcal{C}_{bc} = j_{bc} \mathcal{C}_{bc} \mathcal{C}_{bc} = j_{bc} \mathcal{C}_{bc} \mathcal{C}_{bc} \mathcal{C}_{bc} = j_{bc} \mathcal{C}_{bc} \mathcal{C}_{bc}$

The input admittance due to Gic is thus

1 = Jw Grc (H gm RL)

This is equivalent to replacing G'c with (1+3mRc) & that is parallel to Ge.



if gmis too small transistor is not amplifing.

RF Page 51

$$= -g_{m}R_{L} \frac{r_{2}}{r_{3} + (R_{5} + Y_{6})} + \int W C_{eff} K_{2} (R_{5} + Y_{6})$$

$$= -g_{m}R_{L} \frac{r_{2}}{(r_{2} + R_{5} + Y_{6})} (1 + \int W C_{eff} \frac{1}{2} (R_{5} + Y_{6}) \frac{1}{2} + (R_{5} + Y_{6})$$

$$bt us befine Ref = (Y_{6} + R_{5}) F_{2} + (R_{5} + Y_{6})$$

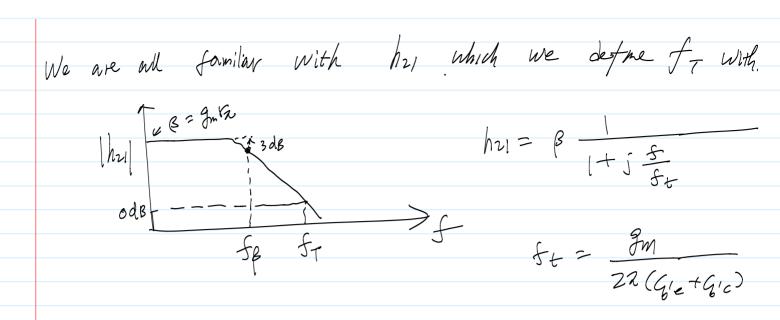
$$V_{5} = -g_{m}R_{L} \frac{r_{2}}{12} + (R_{5} + Y_{6})$$

$$V_{7} = -g_{m}R_{L} \frac{r_{2}}{12} + (R_{5} + Y_{6})$$

$$V_{7} = -g_{m}R_{L} \frac{r_{2}}{12} + (R_{5} + Y_{6})$$

$$V_{7} = -g_{m}R_{L} \frac{r_{2}}{12$$

Reall: Reft
$$\stackrel{\triangle}{=}$$
 $\frac{(r_b + R_S)r_b}{(r_a + (r_s + r_b))}$ $\stackrel{\triangle}{=}$ $\frac{(r_b + R_S)r_b}{(r_b + R_S)}$ $\stackrel{\triangle}{=}$ $\frac{(r_b + R_S)r_b}{(r_b + R_S)}$ $\stackrel{\triangle}{=}$ $\frac{r_b}{r_b}$ $\frac{r_b}{r_$



Numerical example of a medium current RF transistor

Sunday, November 04, 2012 2:43 PM

Medium Current RF Transistor, Ic = 1 om A

Say fr=5642, B=100, G'c=1pF. Vb=1052.

$$g_{m} = \frac{I_{c}}{V_{t}} = \frac{lom A}{25mV} \qquad \frac{l}{g_{m}} = 2.552 \quad (also called)$$

$$r_{s} = I_{g} \qquad or \quad r_{e} = 2.552 \qquad r_{e}$$

$$\frac{1}{g_m} = 2.5 \, \Omega$$

$$=\beta\cdot\frac{1}{gm}=25052$$

From
$$f_t = \frac{g_m}{2a \left(g_{ie} + G_{ic} \right)}$$
, $G_i = f_{ie} + G_{ie} = \frac{g_m}{2a f_t}$

$$GetG_c = \frac{g_m}{2aft}$$

$$= \frac{1}{27.5} = \frac{12.6}{7} = \frac{12.6}{12.6} =$$

For S-para,

$$= (1 + \frac{50}{2.5}) \cdot 1 pF + 11.6pF$$

$$= 32.6 pF$$

pay attention to this term.

your Cett >> Chet Gic (what is indicated by ft)

even if Gic is only IPF.

$$|S_2| = -2 g_m \cdot 50 \frac{1}{150 \text{ Get}} \frac{1}{150$$

at low frequency

$$5u = -2 \frac{1}{2.5} = -32.25$$

at high pregnany it will stop by 20dk/seade like in $|h_{21}|$, as

You can befine Szi cut off if you want

3 de fregueno of Su

$$f_{3}dB = \frac{1052}{22 \left[(1+g_{m}R_{L}) G_{c} + G_{e} \right] (r_{b} + R_{5}) r_{c}}{32.6 \times 10^{-12}} = \frac{1052}{1052} r_{b}$$

= [0/ MHZ

Numerical Example of Lower Current RF Transistor

Sunday, November 04, 2012 2:45 PM

$$f_t = 56H2$$
, $\beta = 100$, $I_c = 1mA$. $G_1c = 0.2 pF$

Now
$$\frac{1}{gm} = \frac{V_t}{I_c} = \frac{25mV}{1mA} = 2552$$
 For typical $1mA$ device

$$G_{ie} + G_{ic} = \frac{g_{m}}{2aft} = 1.26 pF$$

1 1 1 1

$$= \frac{2500 + 100 + 50}{27 \times 1.66 \times 10^{-12} \times (100 + 50) \cdot 2500}$$

$$= 678 MH2$$

$$= 2 \cdot 9m \cdot 50 \frac{72}{11 + 100}$$

$$5_{21}|_{f\to 0} = -2 \cdot g_m \cdot 5_0 \frac{r_2}{r_2 + r_6 + 5_0}$$

$$=-2\cdot\frac{50}{25}\frac{2500+100+50}{2500+100+50}=-3.77$$

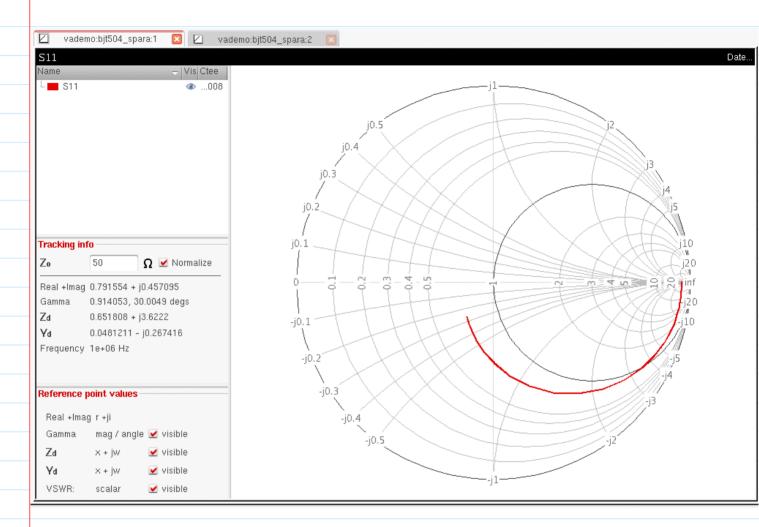
13F625A is such a fransister.

low frequency
$$521 = -2 gnRL \frac{12}{12 + 16 + 50} = -2 gnRL = -2 \frac{20}{re}$$

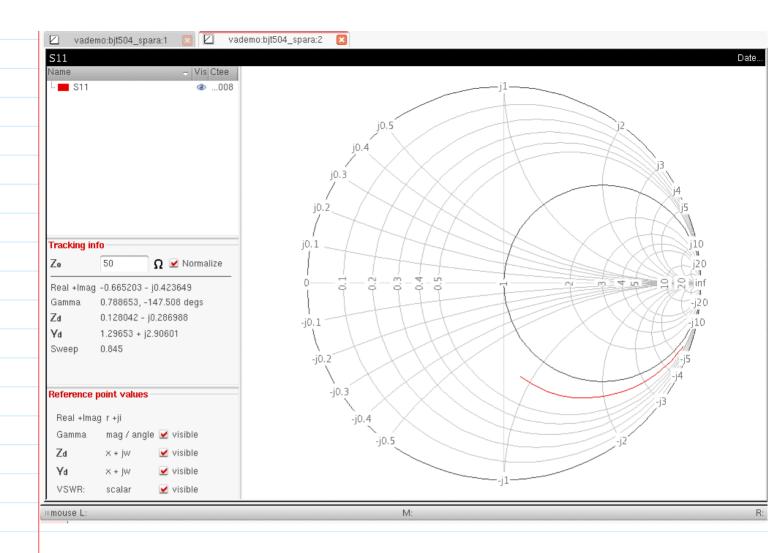
$$f_{3d8} = \frac{(7_{6} + 5_{0})}{22 \text{ Ceff}(7_{6} + 5_{0})} r_{R}$$
, $(\text{Ceff} = (1 + \frac{2_{0}}{7_{e}}) \text{ Gic} + \text{Gie})$

Bias dependence	
Sunday, October 28, 2012	7:29 PM

Recall frequency dependence of s11 on smith:

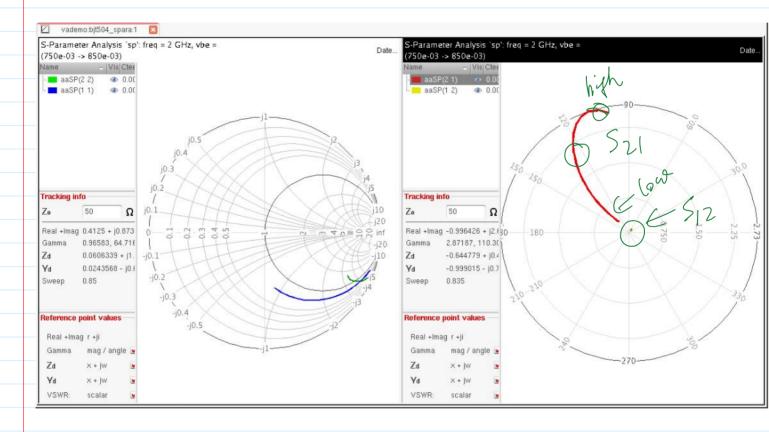


Now let us sweep bias (vbe) for a frequency of 2GHz - a useful frequency for cellular and wifi



Based on your understanding of s11 and transistor equivalent circuit, can you figure out which end of the curve is higher vbe?

Vbe dependence of all s-parameters, see if you can tell what is what, and which end is low vbe which end is high vbe based on your understanding:

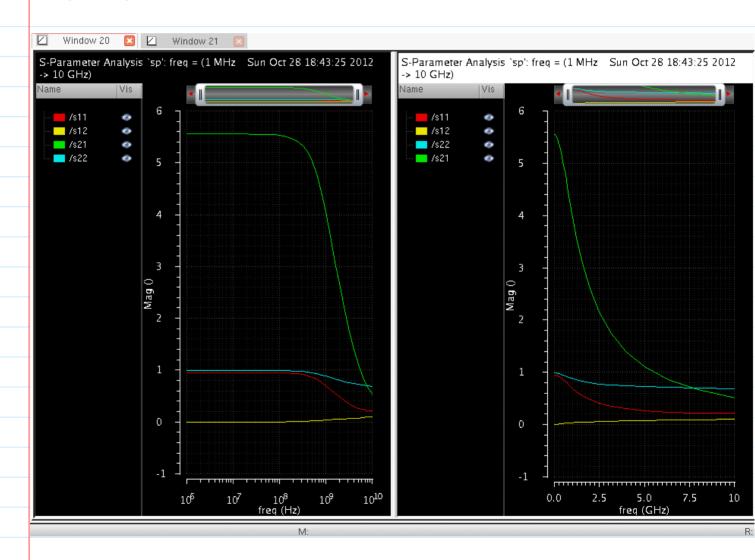


Magnitude of all s-parameters vs frequency

Sunday, October 28, 2012 9:19 PM

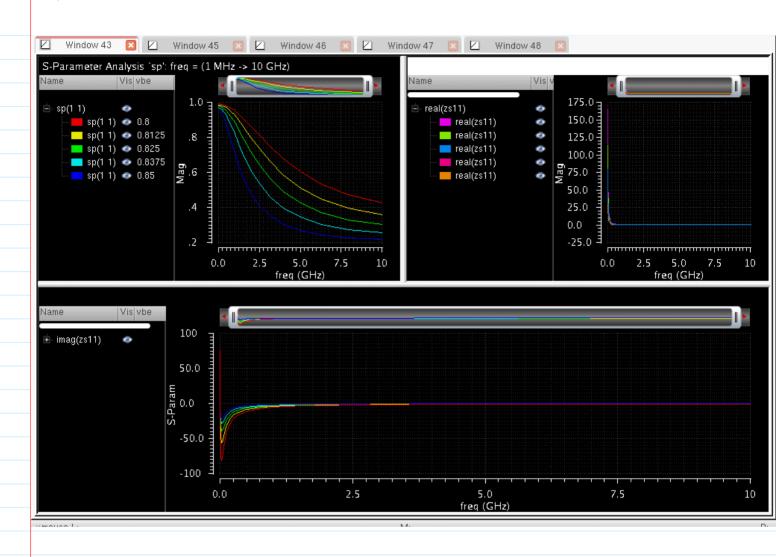
At useful biases (not too far from peak ft.), if transistor is not too small, the magnitude of all s-parameters vary with freq like shown below.

Here I'll first show the values of all s-parameters without taking db20, but I'll use both log scale and linear scale for frequency,



Your mag S21 can be easily larger than "1" at low frequency, and in general decreases with increasing

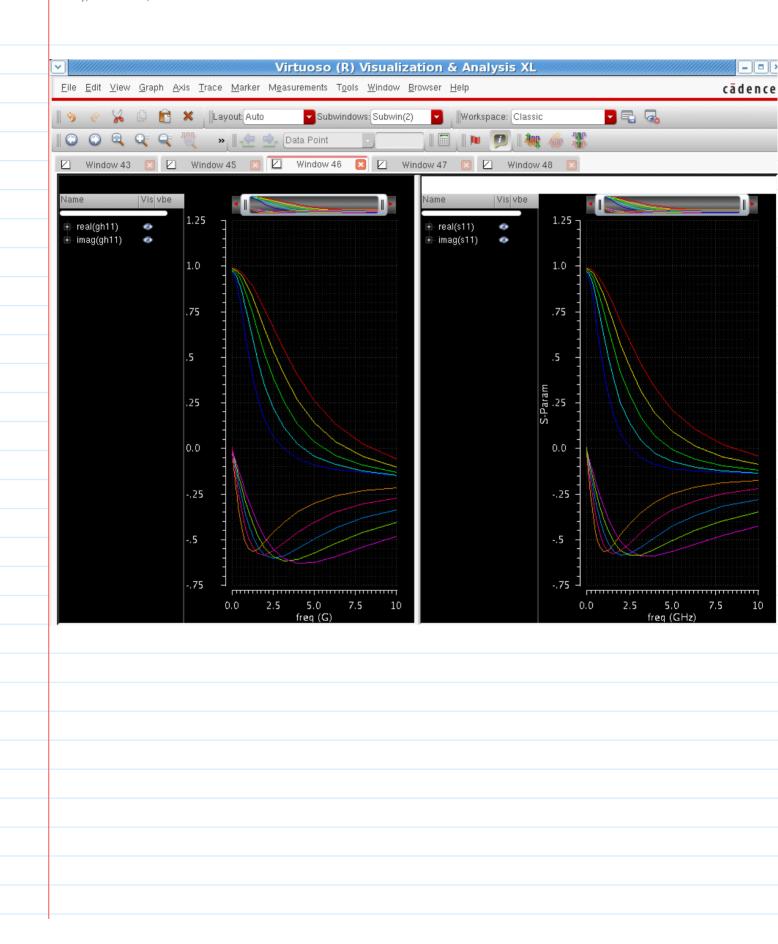
frequency
Your mag of s11 and s22 should in general be less than
"1" - on smith chart, it is within the r = 0 circle.
Your mag s12 should in general be very small, much
smaller than s21.



Frequency dependence with bias sweep Sunday, October 28, 2012 10:37 PM						

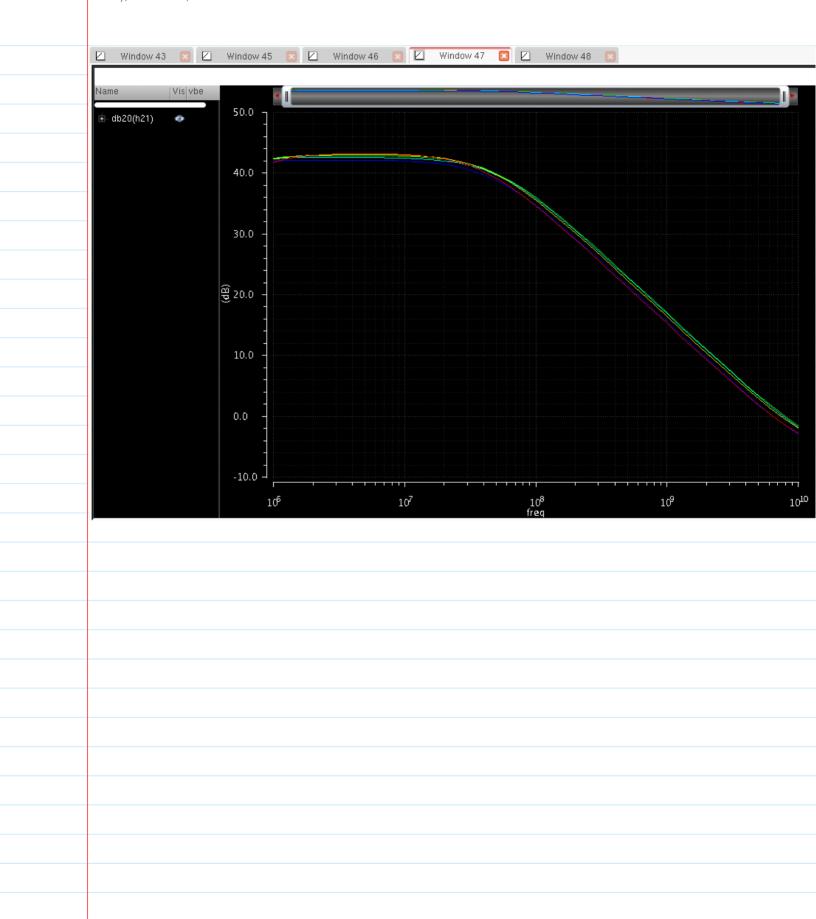
Gamma(h11) and s11

Sunday, October 28, 2012 10:37 PM



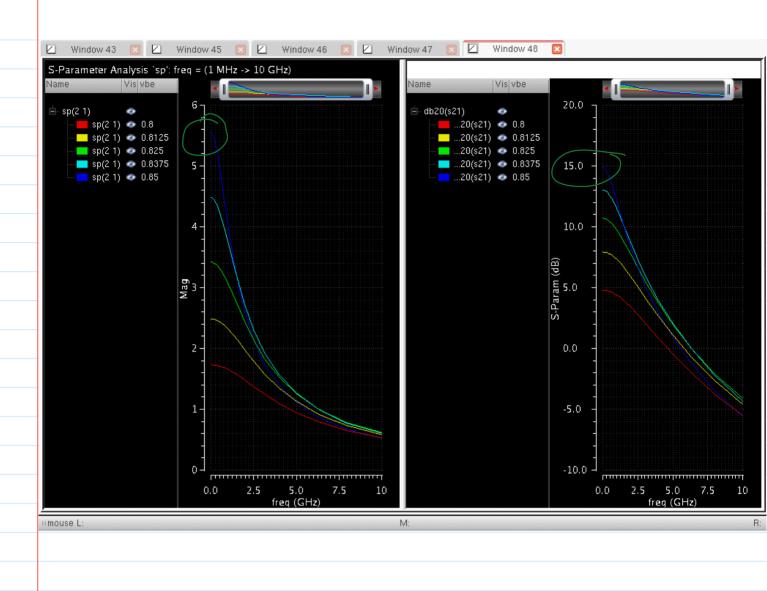
db20(h21)

Sunday, October 28, 2012 10:39 PM



S21 and db20(s21)

Sunday, October 28, 2012 10:39 PM



Transistor sizing - how to choose my transistor size

Tuesday, October 30, 2012 9

9:37 AM

For the same VBE, current density is the same.

If you put two identical transistors in parallel, for the same voltage, all currents are doubled.

So all conductance/admittance will be doubled (2x) - e.g. all of your y-parameters.

All resistances/impedances will be halved (1/2x) - e.g. h11, all the your z-parameters.

If you heard of noise matching admittance Yopt and noise matching impedance Zopt, they also obey the same rule.

All current gains remain the same, e.g. h21 which is a function of current density, or VBE.

For bipolar transistors, changing size typically means changing the emitter length and/or the number of emitter fingers.

Of course, it is possible to use parallel connection of multiple unit transistors.

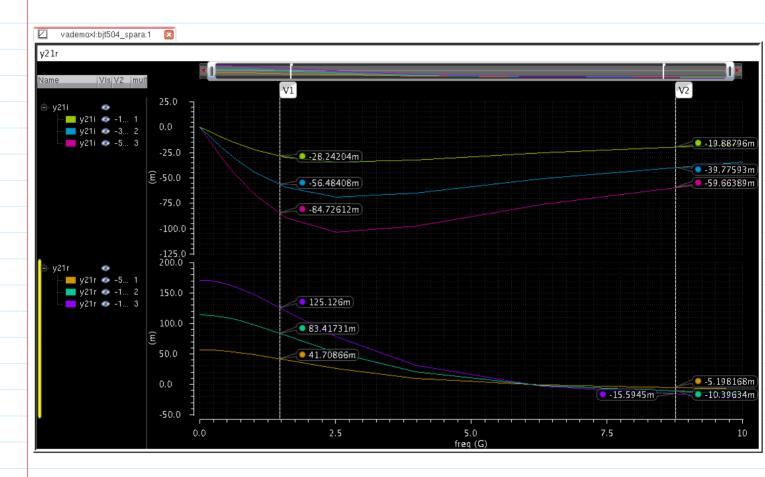
Your s-parameters, however, do not have a simple

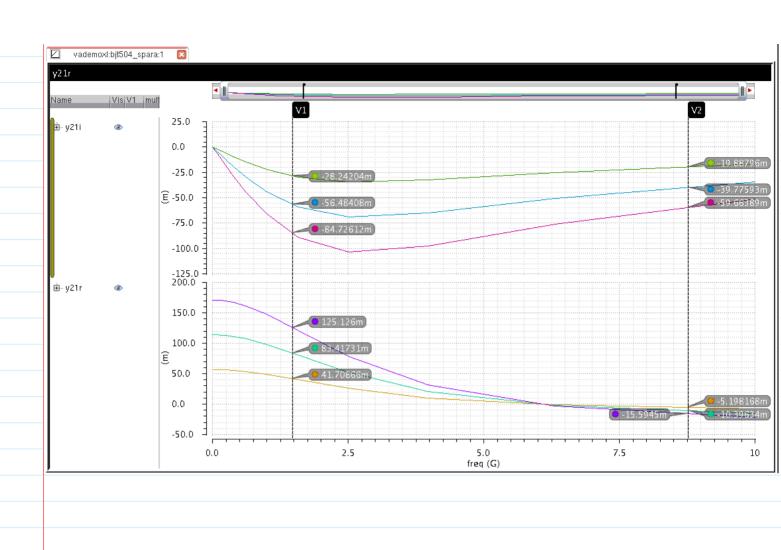
scaling rule, simply because it involves not only voltages
and currents, but also a reference impedance Z0.
So if you have a device that is too small or too large, its
s11 can be too close to "OPEN" circuit or "SHORT" circuit
in comparison to Z0 (50ohm).
You always want to measure devices with "reasonable"
size, meaning, not too far away from 50 ohms.

Real(y21) imag(y21) scaling example

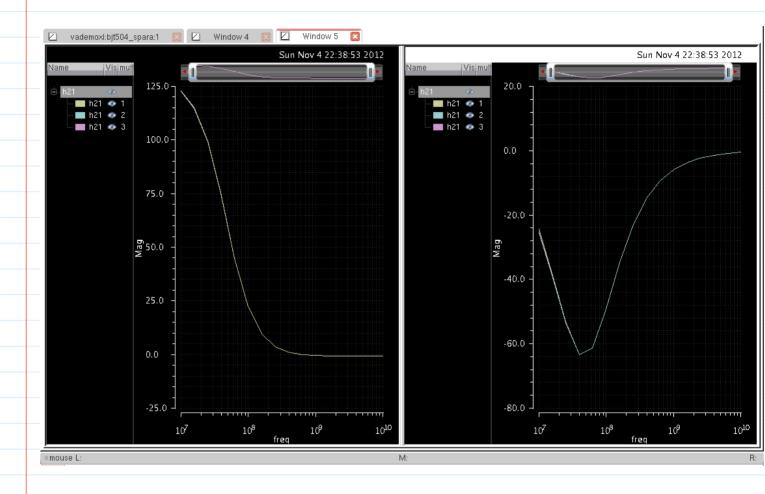
Sunday, November 04, 2012 10:23 PM

Same VBE, we set the "mult" parameter of our verilog-a model. Mult=2 is equivalent to 2 devices in parallel, mult=3 means 3 in parallel.





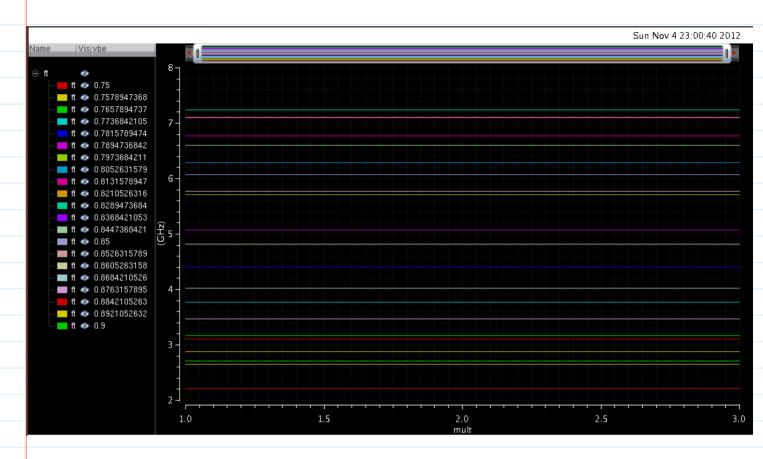
Same VBE. Mult=1,2,3, note that all three devices have the same h21.



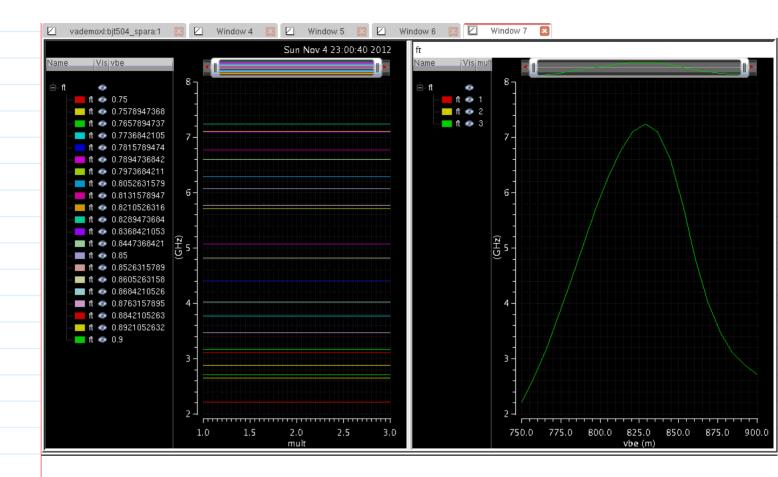
ft.

Sunday, November 04, 2012 11:06 PM

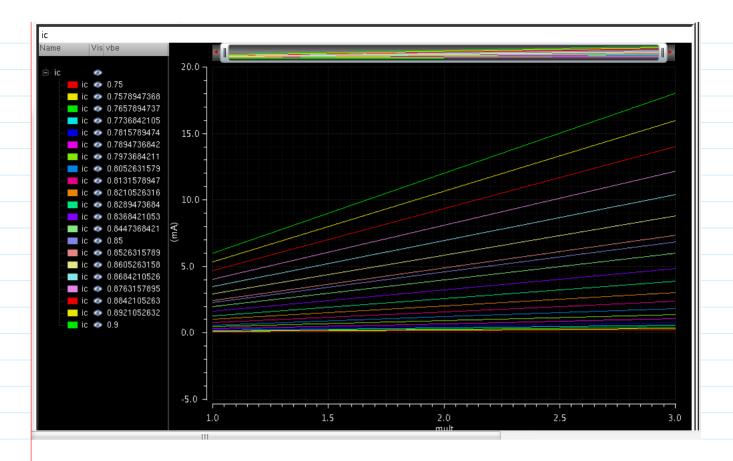
We can repeat this for many other VBE's:



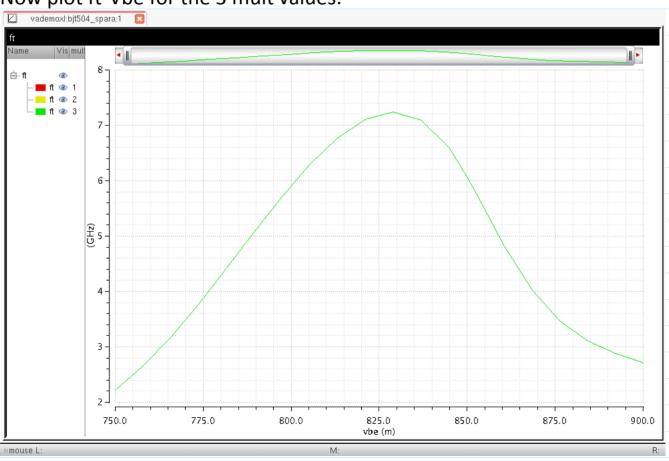
If we plot out ft.-VBE for the three mult values:



We must realize that for the same VBE, all of the currents increase linearly with multi.



Now plot ft-Vbe for the 3 mult values:



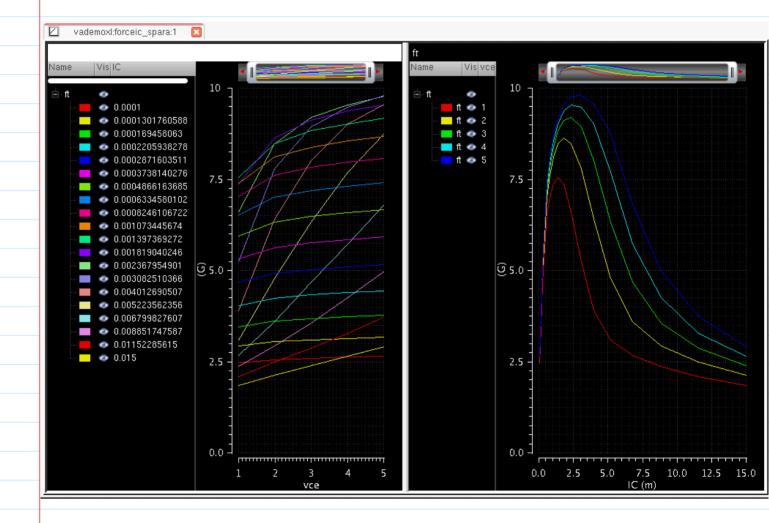
Ft-IC curve for multiple VCE

Sunday, November 04, 2012

9:58 PM

In general, for the same IC, a higher VCE leads to a higher ft in high injection.

This is primarily due to suppression of high injection effect.



How to use IC instead of VBE as design variable

Monday, November 05, 2012 9:52 PM

Often you want to use current as design variable. How can we achieve this in circuit simulation?

What we have done is to use "YvsY" in plotting. This does not always work.

Say you have to fix current at 3mA, and want to find an optimal size that will give say lowest minimum noise figure.

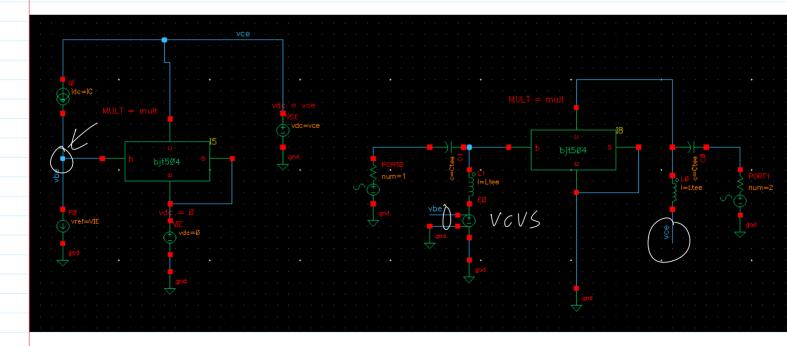
You may / can then need to sweep this current.

The circuit below allows you to do just that.

On the left is a circuit that produces the VBE required for a given IC - which is specified using a current source (I0).

Think about how this circuit works.

Then this VBE is applied to our s-parameter measurement circuit's base-emitter voltage dc bias, via a voltage controlled voltage source (E0).



This can be a very hard to understand circuit.

A famous circuit in analog is the "Wilson" current source. It is a result of a competition between two analog designers, Gilbert (yes the same person in Gilbert mixer) and Wilson, in the 60s.

It was about trying to come up with a better current source using only 3 transistors.

Wilson won.

Google "Wilson current source" for more info.

We cannot directly use that source as it still does not allow us to set VCF.

So instead of using a real current mirror at the bottom, we here use just an ideal current mirror using CCCS - current controlled current source, this way, we can use "zero" voltage for our current "sensor".

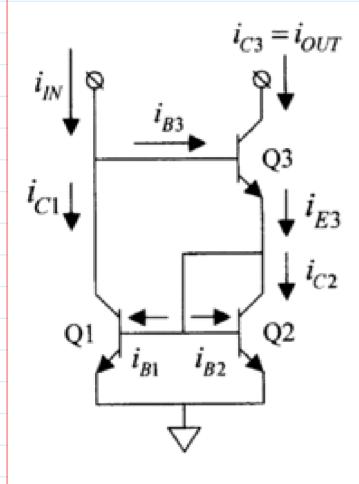
There are a few other ways to make the circuit recisely producing an IC that is the same as our IC input current source, but I have had a very hard time getting convergence.

I once got it to converge, but then lost it quickly.

But for our purpose, this works almost perfectly. There is a small error of 2*IB, which means 2/beta in percentage.

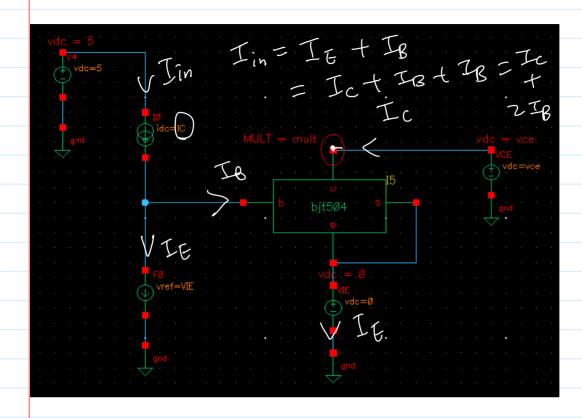
Fixing VCB and IC at the same time, however, is much easier.

http://en.wikipedia.org/wiki/Wilson current mirror



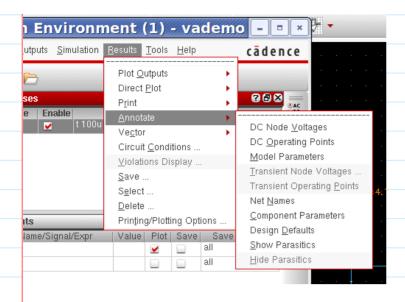
Circuit that produces the right amount of IC at given VCE

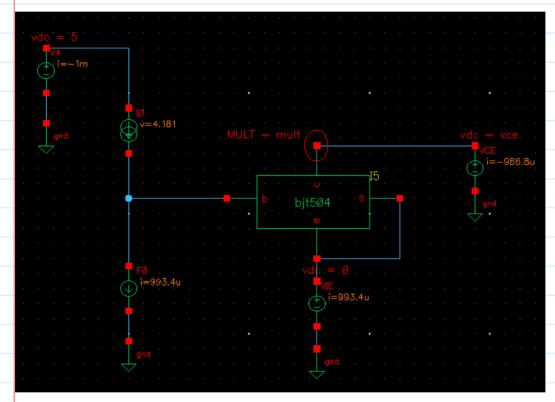
Wednesday, November 07, 2012 9:15 PM



_ Name	Value	
1 IC	1 m	Т
2 mult	1	
3 vce	3	

Dc solution:

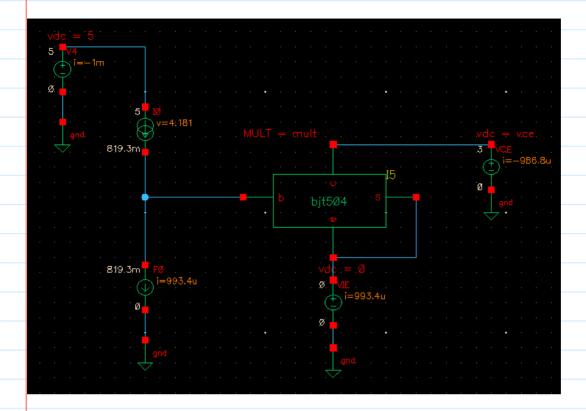




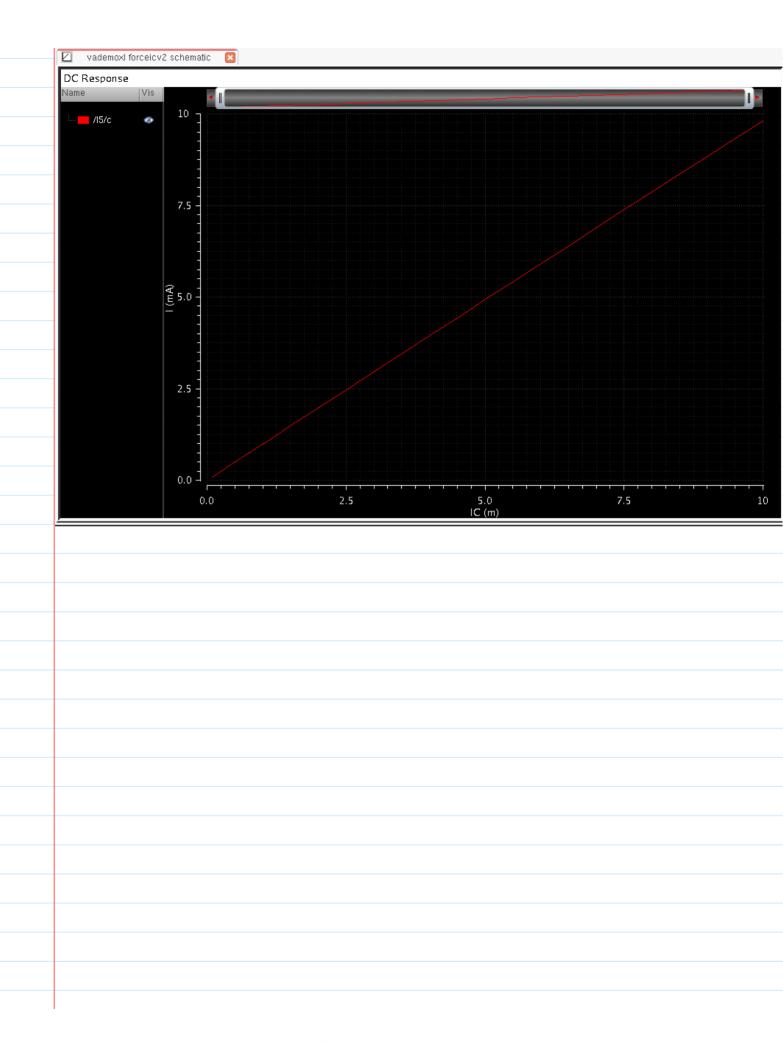
You will find that for an input "IC" (IO current) of 1mA - (V4 current), and VCE of 3V, we obtain an actual IC (flowing through VCE) of 986.8uA.

For voltage source, if the current shown is negative, it means current flows out of the "+" terminal.

Now add dc voltages:



Now let us sweep the "IC" design variable, and plot out the actual collector current at the "c" terminal of bjt504.



Transistor noise parameters and LNA design - the short version Monday, November 12, 2012 5:18 PM
I'll present here a short version of this complex topic.
We will use a fixed biasing current optimization as an
example and show how to do design using cadence.

Noise parameters - short version

Monday, November 12, 2012 5:12 PM

Noise parameters

Noise figure

NF = 10 logio F

F: noise fa

Ts=Grs+jBs

OF -> minimum Finin when to = ts.opt

Noise matching thru transistor sizing

Monday, November 12, 2012 5:16 PM

	50	I a scale device size such that
Noise	matching Si	
	25= 25.0pt	/ Rs.opt = Rs
L _B	7 tin	2 chose L for
10004		w-L = Xopt.
\$ R3=50 SL	'	W L /Kopi .
्रे <i>ง</i> ड		I P of tixcopt
]		Zs,opt = Rs,opt + j Xs,opt
		- Tsopt

Roise matching + impedance matching

Adding emitter inductor's impact

Monday, November 12, 2012 5:12 PN

Now consider adding LE - emitter inductor

The new two port device Combo

NFmin ~ NFmin

R Combo device

Rs. opt ~ Rs. opt

device

through linear circult analysis => Rn ~ Rn

Combo device

Xs. opt ~ Xsopt ~ WI

LE Can be chosen to produce real part Zin

RelZin = WT. LE = Rs

Simultaneous noise and impedance matching

Monday, November 12, 2012 5:20 PM

Can we possibly achieve noise matching and impedance matching at the same time without increasing noise figure? - Yes.

Now consider adding LE -emitter inductor

The new two port device to the combo

Normin & Normin

Respect & Respect

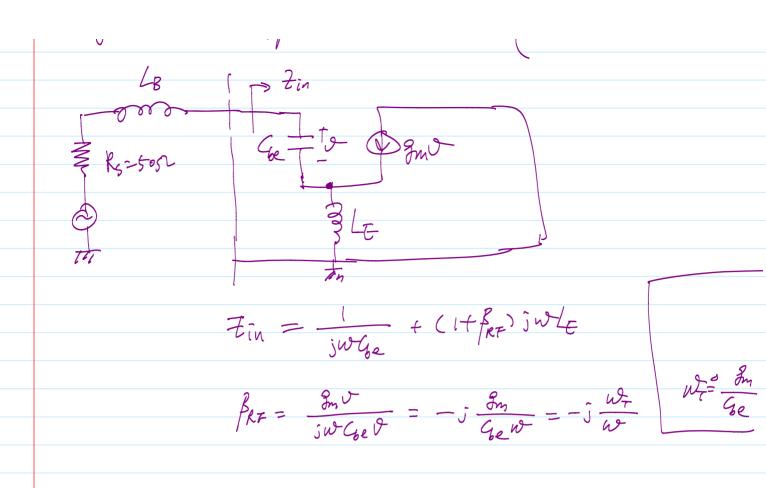
Combo

Le can be chosen to produce peal part Zin

Relizin] = WT. LE = Re

So the real part is impedante matched (7-match)

Luckily, the Xs, apt is also the (Xin) & do



Thus:
$$\overline{Zin} = \frac{1}{j\omega Ge} + j\omega L_{\xi} + \omega T_{\xi}$$
 $L_{\xi} = \frac{R_{\xi}}{2zf\tau}$
 $L_{\xi} = \frac{R_{\xi}}{$

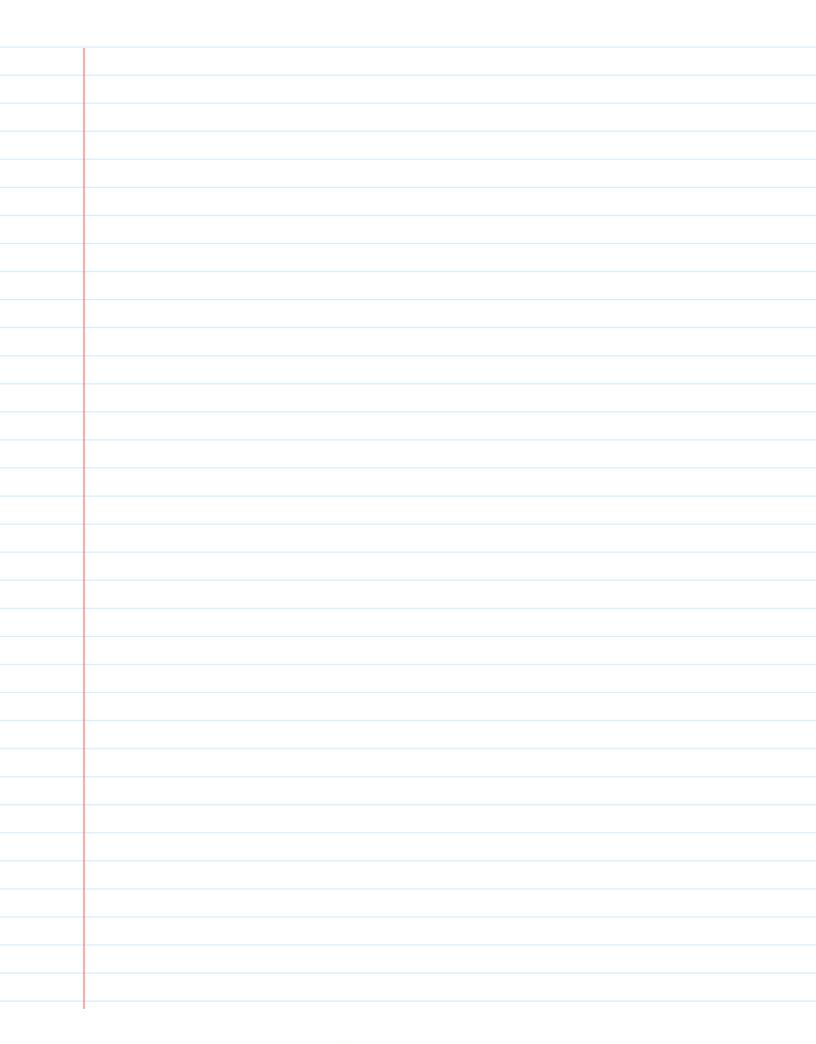
* Even if these assumptions are not always valid.

We can tolerate some noise mis-match as long as

it is not too far off and Rn is small

* The insight can still be used at least to

noise moth the real part, t injectance mothing.





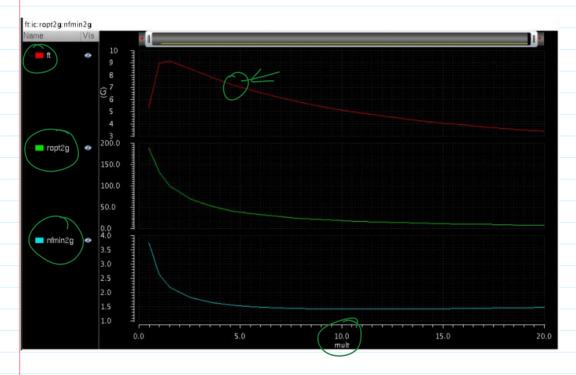
Case Study of Device Circuit Interaction - Optimal Sizing Under Fixed current (power consumption) for RF Low-Noise Amplifier Design

Sunday, November 11, 2012 1:19 PM

A very important issue in IC design is to optimize size of transistors.

For instance, in RFIC design, e.g. the LNA, amplifier transistor's size can be optimized.

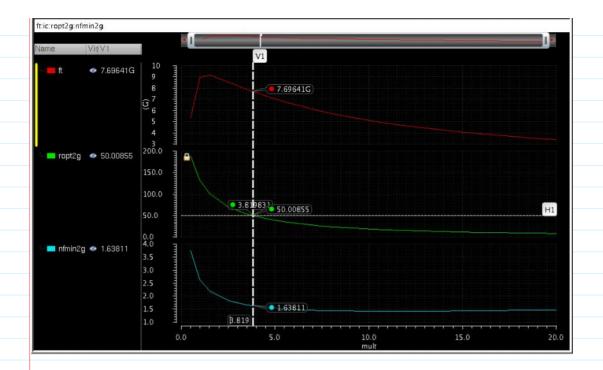
Consider 3mA, 3V VCE, for the same bit we have been using, at 2GHz,



We sweep "mult" and plot out ft and ropt2g as well as NFmin2G versus Mult.

Let us find the "mult" that gives us a 500hm ropt2G. The ft. is still

7.7GHz, not too bad, NFmin2g is 1.64dB, almost near the minimum one can have for this current value.

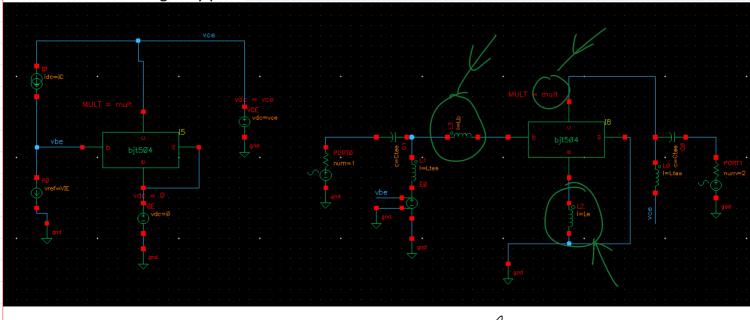


So we set "mult=3.82",

Next, we need to produce an input impedance equal to source impedance (source side impedance matching) for several reasons

in RF LNA design. This can be achieved by placing an emitter degeneration inductor Le, which produces a real part (50 _____Ohm),

and modifies the imaginary part.



Then an base inductor Lb can be adjusted to make the total imaginary part zero.

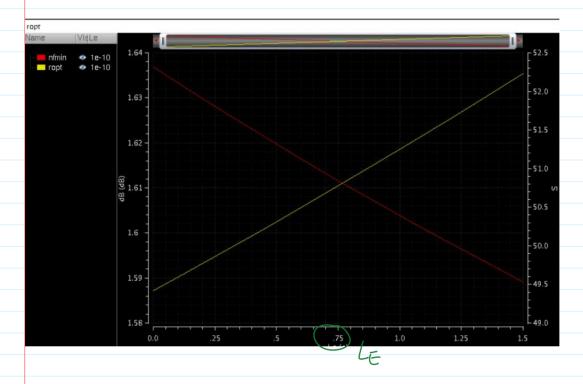
With the "mult" (size) determined above, we sweep emitter

inductance Le from 0 to 2nH,

do

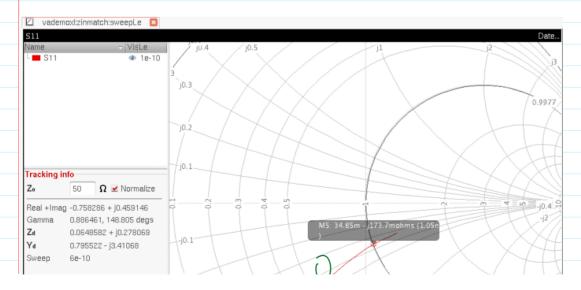
We plot out S11 and see that as we sween Le, Nfmin and Ropt

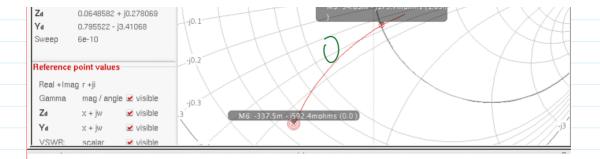
not change for all practical purposes (tiny bit),



However, the real part of zs11 (or Zin for 50ohm load) increases,

of course the imaginary part increases some too,

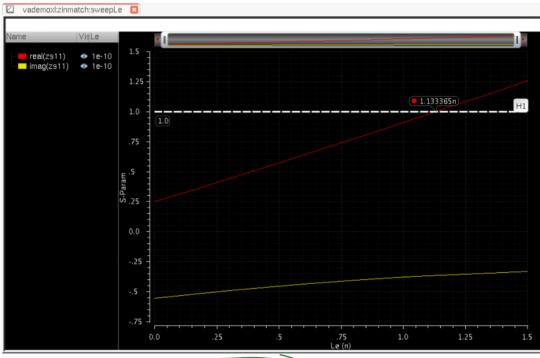




Better yet, we can do a transform from s11 to zs11 (see previous

notes if doubts), and plot out the real and imag of zs11 versus

Le:

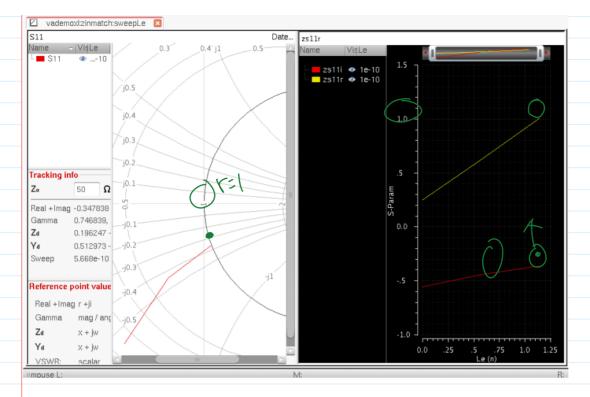


We can label the Le=0 and Le=1.136 nH points to see the difference - this can be proven from circuit analysis, that is, adding emitter inductor can produce a real part in the input impedance at RF.

This applies to MOSFET too, and is used in both RF SiGe, III-V and

CMOS LNA designs.

Modify your Le upper limit in sweep to 1.1336nH as found above:



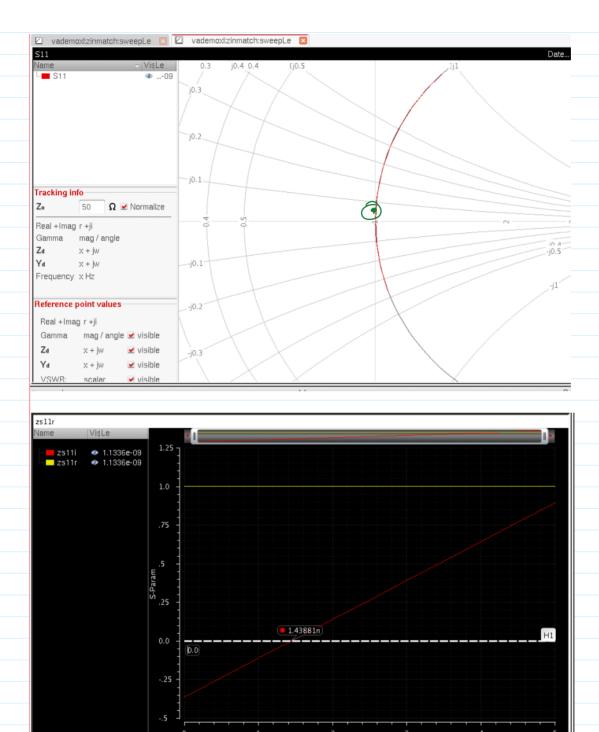
We see from both Smith and zs11r plots that we can indeed produce a 50ohm real part of input impedance by adding proper

amount of emitter inductance.

Next let us set Le = 1.1336nH and sweep Lb to move S11 to center of Smith, or to make the imaginary part of Zs11 zero.

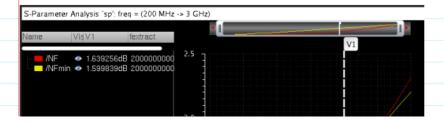
Now sweep Lb, observe that zs11r (real part) does NOT change,

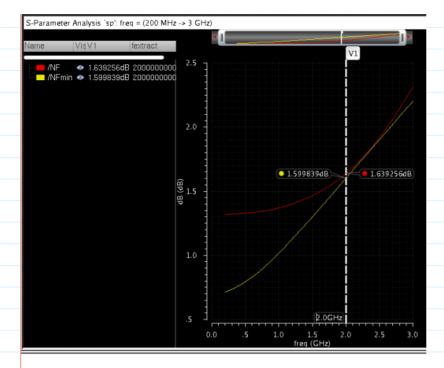
while zs11i (imag prt) changes.



The Lb value required is 1.438 nH. Now we have determined the size (mult), base inductance Lb and emitter inductance Le.

Now put all the values in, do a freq sweep from 0.2 to 3GHz,

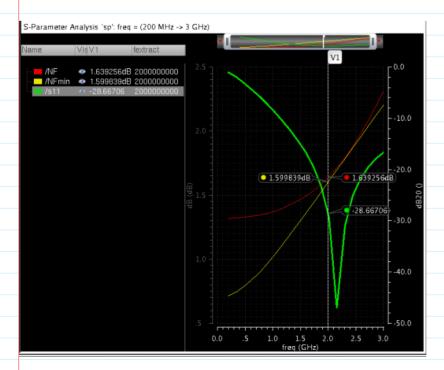




We see that the noise figure is very close to Nfmin at 2GHz, and this is also very close to Nfmin of the transistor alone at the same

transistor size and bias.

Now add S11,



The s11 dip does not happen precisely at 2GHz, which is normal

considering that we did not use optimizer. We can of course make

the dip center at 2Ghz in design. The L's and their changes will eventually make the measured S11 worse than simulated / ____ designed.

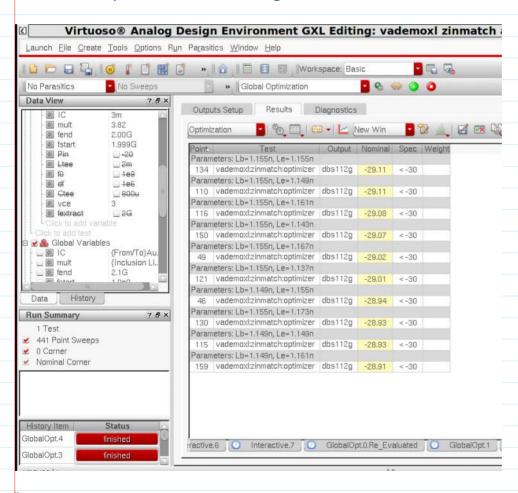
Optimization in Cadence for impedance matching is not easy to do

compared to say in ADS.

One thing I do is after I have found a solution using my design procedure, I'll run the optimizer near the solution. Without that,

optimization simply fails.

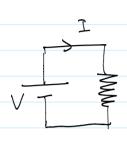
Below is an optimization done using ADE-GXL:



GlobalOpt.4 stopped because ADE GXL cannot find a better design point. Number of points completed: 225 Number of simulation errors: 0

GlobalOpt.4 completed. Current time: Sun Nov 11 16:35:23 2012

noise



$$I = \frac{V}{R}$$
 I + noise

* actually only the de component

* There is noisy current even if V=0

i = Ide + in(t)

* in(t) =0 average is zero

x instant value is unpredictable

X In noise work, we talk about the FMS value

(Foot mean square). In, rms = Jin

for voltage In. rms = Jon

If there are two sources of noise

e.g in, in. $\overline{i_n^2(t)} = \overline{i_n(t)} + \overline{i_n(t)}$

+ 2 in (t) in t

X In measuring noise, the amount of noise depends on the band width of the measuring system

a very namew band width of is typically involved with red at f. as $csf \to o$ $\frac{\overline{n^2r^4}}{\Delta f} \to \frac{S_{\pm}(f)}{\Delta f}$ $\frac{psd}{psd}$ $\frac{psd}{psd}$ $\frac{psd}{psd}$ $\frac{psd}{psd}$ $\frac{psd}{psd}$ $\frac{psd}{psd}$ $\frac{psd}{psd}$

for voltage Sv · v2/HZ

The isgrt of the PSD is also often used.

 \pm The total mean square current from f, to fz is $\frac{f_2}{f_n}(f, \rightarrow f_2) = \int_{f_1}^{2\pi} (f, \rightarrow f_2) df$

* Thermal noise

$$\frac{1}{2} \int_{R}^{\infty} V_{h} S_{h} = 4kTR$$

$$= \frac{4kT}{R}$$

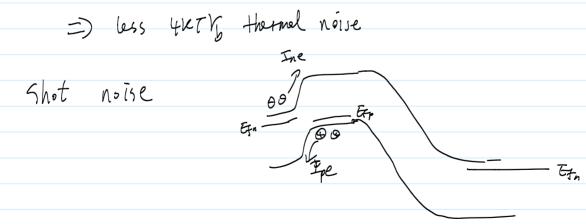
$$= \frac{4kT}{R}$$



Sin are independent of f. thus "white". thermal noise in site HBT Surb = EXTT Sure = 4KT Ye Sure = 4KTYC

To is at the input, and most important Sife HBT allows high base doping—due to base Egreduction,) less to than Si BJT for the same

= less the thermal noise



Carriers crossing a barrier independently

each passing of e or h Optimers a 2 charge

The flow of "9" obeys Poisson statistics. \Rightarrow Math (statistics yields \Rightarrow Sine = 22 Ine = 29 Ic

Sipe = 29 IF

it is called "Shot" Noise

Ine = Ic

Ic current has 22 Ic noise PSD

Is - 22 Is noise PSD

ofun PSD is left out

SIB = 22 Is - B Site incremes B

so site HBTS have

less SIB

A good first order White noise ckt

YE HKT TO

22 Is D 22 Ic

* Keep in mind that the 22 To or 22 To shot noise assumes that VBF and VCF are "fixed" ideal voltage sources, i.e. ac short circuit conditions

If we have finite source / lond resistances, the Sib Sic measured would differ *

* In noise work. we are Mostly interested in the *

* Noise source.

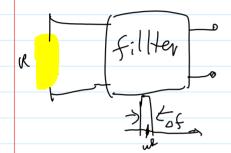
* Short circuit noise currents are such noise sources

Thermal noise (Johnson noise)

Wednesday, September 05, 2012 4:56 PM



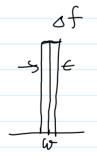
D → 102 = 4k7Ksf mean square



bandwish

The power of the noise output where is

the same as that of a sin wave



wheing center steg, of the filter

An is zero to peak.

$$\frac{1}{2} \frac{1}{2} = \frac{4n^2}{2} = 4kTR\Delta f,$$

$$\frac{1}{4} \frac{1}{\sqrt{2}} = \frac{4n}{2} = 4kTR\Delta f,$$

It is very important to keep this point in mind as we proceed, because it simplifies noise analysis to regular ac circuit analysis.

That is, we can treat noise at a given frequency, for a small band width Delta f, as a sine wave as far as noise power is concerned.

$$4$$
 of ten, $\frac{\mathcal{Y}_{n,rms}}{\partial f}$ or $\frac{\mathcal{Y}_{n,rms}}{\sqrt{\log f}}$ is used in calculations.
 $S_{v} \stackrel{\circ}{=} \frac{\mathcal{Y}_{n,vms}}{\partial f} = 4kTR$ $R = |kn|$

$$T = 290k$$

$$S_{v} \stackrel{\circ}{=} \frac{\mathcal{Y}_{n,vms}}{\sqrt{\log f}} = \sqrt{4kTR}$$
at $T = 290k$, $S_{v} = 4nv \cdot \sqrt{3Ha}$ for $R = |kst|$

$$S_{v} = |l \cdot b| \times 10^{-17} \text{ V/Hz}$$

RF Page 112

Example 1:

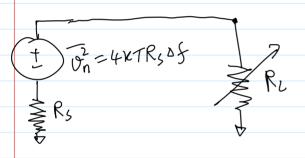


Assume that k = **Boltzmann constant** = **1.38066** x 10-23 J/K. Bandwidth delta f is 1Hz.

7=290K

Apply the equivalence you just learned above to find out the maximum amount of thermal noise power that can be delivered to the noiseless load for any possible RL values. Then convert that number to dBm.

Is your result dependent on the value of Rs?

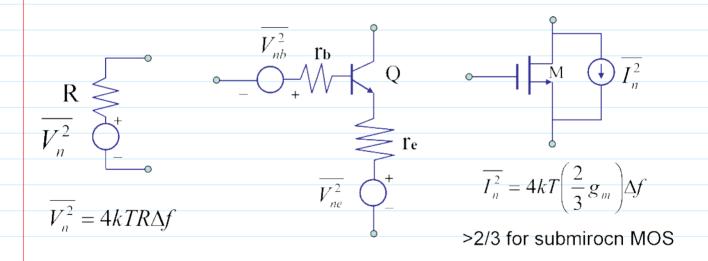


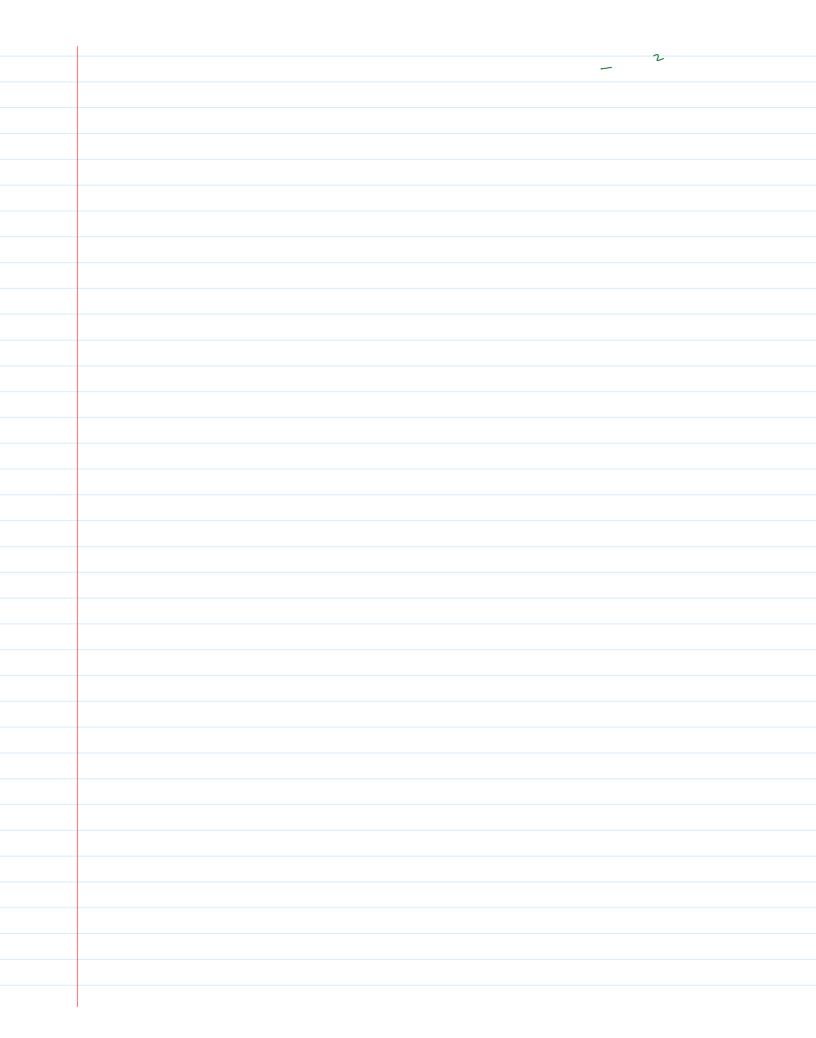
Rs is fixed. When R = Rs. PRI is maximized

Rs
$$\frac{1}{\sqrt{N_{n,rms}}} = \frac{V_{n,rms}}{\sqrt{N_{n,rms}}} = \frac{1}{\sqrt{N_{n,rms}}} = \frac{1}{\sqrt{N_{n,rms}}$$

* Golution Proise available = KT. Of

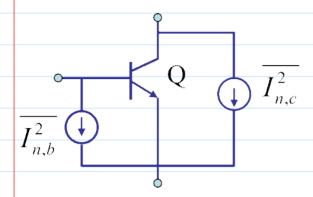
-174+10*log10(200e3)=-120.9897000433602





Bipolar transistor shot noise

Wednesday, September 05, 2012 5:56 PM



$$i_{bn} = \sqrt{2qI_B}$$

$$i_{cn} = \sqrt{2qI_C}$$

$$\overline{I_n^2} = 2qI\Delta f$$

$$i_{cn} = \sqrt{2qI_C}$$

$$\overline{I_n^2} = 2qI\Delta f$$

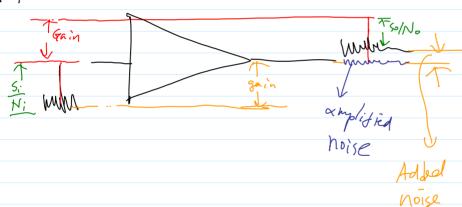
noise figure:

purpose: describe how noisy amplifier is



how much noise is a ded by amp?

Detinition



At the input of your amplifier you always have some noise (say from its 50ohm source), and some signal.

You amplifier has no knowledge of what is noise and what is signal, and will amplify both.

If the amp does not add any noise, SNR at input Sin/Nin will be the same as SNR at output Sout/Nout,

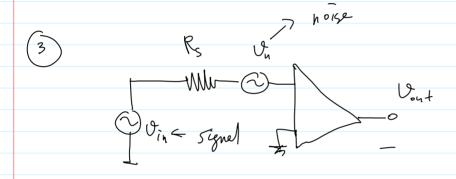
That is a noiseless amplifier - that does NOT exist in practice.

Amplifier adds some noise, so Sout/Nout will be smaller

than Sin/Nin.

Note of we are talking about power

$$\frac{2}{F} = \frac{\sqrt{\frac{1}{2}}}{\sqrt{\frac{1}{2}}} = \frac{\sqrt{\frac{1}{2}}}}{\sqrt{\frac{1}}} = \frac{\sqrt{\frac{1}{2}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}{2}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}{2}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}{2}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}{2}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}{2}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}{2}}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}}}{\sqrt{\frac{1}}}} = \frac{\sqrt{\frac{1}}}}{\sqrt{$$



in terms of power

So once we know Nadded. Fis known Nadad: output noise generated by Amp Ningain: output noise generated by the Source 50 F can also be written as Output noise due to Amp

F=1+ Output noise due to Source

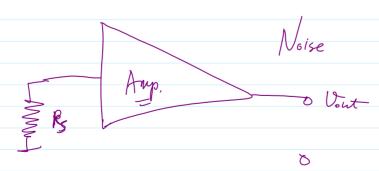
* Rs has a lot to do with Nadded. esay to understand Rs & Pin if Rs = 0

In will be shorted. =) no output

due to Days. lout no output due La Ps

if
$$R_s = 1$$
.

Nadded = $(1n) \cdot 3^2 \cdot R_{load}$



2nd stage!

Nodell = (F2-1). Nin/o 92

What about 3 stages? Just combine the first 2 stages with a gain of G1*G2, then apply the above procedure again:

$$(F-1) |_{total} = (F_1-1) + \frac{F_2-1}{G_1}$$

$$-\frac{G_1}{F_2-1}$$

$$-\frac{G_2}{F_2-1}$$

$$-\frac{G_3}{F_2-1}$$

$$-\frac{G_4}{F_2-1}$$

$$-\frac{G_4}{F_2-1}$$

$$-\frac{G_4}{F_2-1}$$

$$-\frac{G_5}{F_2-1}$$

$$-\frac{G_7}{F_2-1}$$

$$-\frac{G_7}{F_2$$

O overall NF is dominated by

early stages close to source

The factorial by

Factoria

***** Question:

What is the noise figure of a perfect amplifier that has no noise inside?

$$F_{101} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_{p1}} + \frac{F_3 - 1}{G_{p1}G_{p2}} + \dots + \frac{F_n - 1}{G_{p1}G_{p2...}G_{p(n-1)}}$$

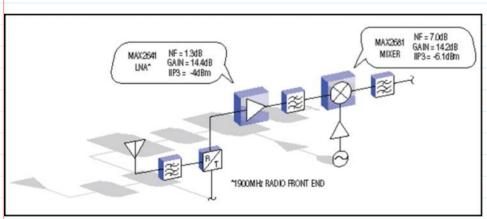
F_{tot} – total equivalent Noise Factor

F_m - Noise Factor of mth stage

G_{pm} - Available power gain of mth stage

Design Example: Typical RF front end circuitry

Implemented with Maxim GST-3 SiGe processing, (f_T) = 35GHz



Long and Comprehensive Version

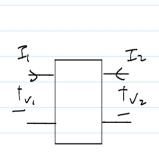
Monday, November 12, 2012 5:17 PM
This will show the long version, with no power
constraint.
This section also has more device relevant material.

Equivalent noise representations

Thursday, September 06, 2012

* There are always equivalent ways of circuit representations

$$\begin{pmatrix} V_1 + V_{n1} \\ V_2 + V_{n2} \end{pmatrix} = \begin{pmatrix} Z \\ Z \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}$$



$$\begin{pmatrix}
I_1 \\
I_{\nu}
\end{pmatrix}^2 \begin{pmatrix}
Y_{11} & Y_{12} \\
Y_{21} & Y_{\nu}
\end{pmatrix} \begin{pmatrix}
V_1 \\
V_{\nu}
\end{pmatrix}$$

$$\begin{pmatrix}
I_1 \\
I_{\nu}
\end{pmatrix} = \begin{pmatrix}
Y_{11} & Y_{12} \\
Y_{21} & Y_{1\nu}
\end{pmatrix}\begin{pmatrix}
V_1 \\
V_{\nu}
\end{pmatrix}$$

$$\begin{pmatrix}
I_{n_1} \\
I_{n_2}
\end{pmatrix} + \begin{pmatrix}
I_1 \\
I_{\nu}
\end{pmatrix} = \begin{pmatrix}
Y_{11} & Y_{12} \\
Y_{21} & Y_{1\nu}
\end{pmatrix}\begin{pmatrix}
V_1 \\
V_{\nu}
\end{pmatrix}$$

SIn1 = 29 TB

for the intrinsic transister

or

without any

or
$$\begin{pmatrix}
I_{n} \\
I_{n2}
\end{pmatrix} + \begin{pmatrix}
I_{1} \\
I_{2}
\end{pmatrix} = Y \cdot \begin{pmatrix}
Y \\
V_{2}
\end{pmatrix}$$
Since = 29 Ic

$$\begin{pmatrix}
 I_1 + I_{nq} \\
 I_2
\end{pmatrix} = \begin{pmatrix}
 I_1 & I_{12} \\
 I_2
\end{pmatrix} = \begin{pmatrix}
 I_1 & I_2 \\
 I_2
\end{pmatrix} = \begin{pmatrix}
 I_1 & I_2$$

=)

Noise parameters

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Noise parameters

noise figure

NF = 10 log 10 F

F: noise factor

15 = Gs+jBs

OF -> minimum Fmin when is = ts. opt

2 [F-Fmin] the deviation depends on Rn Rn determines sensitivity to mismatch

often Topt is used in measurement

子。=5052

Rn. Ts.opt - Es.opt + j Bs.opt

 $R_n = \frac{S_{V_n}}{4\kappa T}$

 $G_{5,opt} = \sqrt{\frac{S_{I_N}}{S_{V_N}} - \left[\frac{I_M(S_{\widehat{I_N}} V_N)}{S_{V_N}}\right]^2}$

from Rn. NTmin. Es. opt

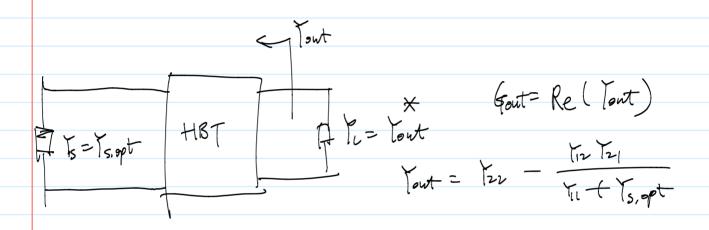
Su Sin and Suy*

can also be calculated o

$$B_{s,opt} = \sqrt{\frac{1}{5v_n}} \left(\frac{S_{In} v_n^*}{S_{Vn}} \right)$$

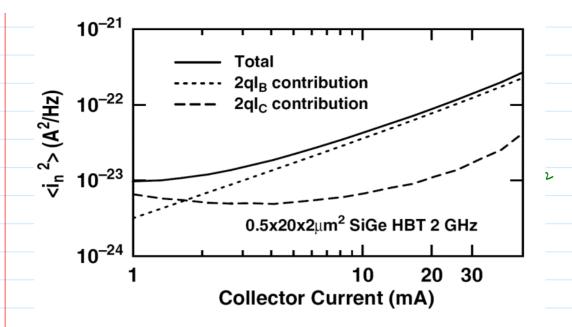
$$E_{s,opt} = -\frac{Im \left(S_{In} v_n^* \right)}{S_{Vn}}$$

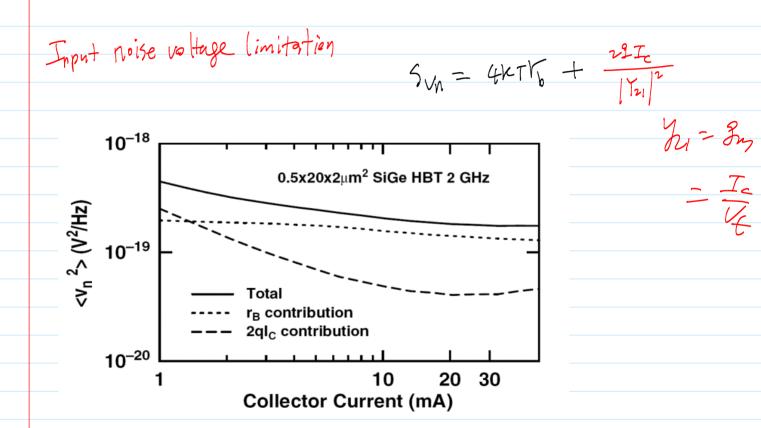
$$F_{min} = \sqrt{\frac{1}{5v_n}} \left(\frac{S_{In} v_n^*}{S_{opt}} + \frac{Re(S_{In} v_n^*)}{S_{In}} \right)$$



Input noise current limitation in site HBTs
$$S_{In} = 22 I_B + \frac{22 I_C}{|H_D|^2}$$

$$= 29 I_C/\beta + \dots$$





Appraches to noise Improvement

P & Ge ordent in base

2) has Ge grading profile optimization

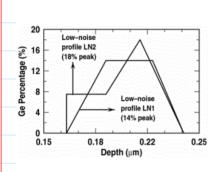
(3) to Hornol cycle limit, total # of boron dose kept in base after fabrication

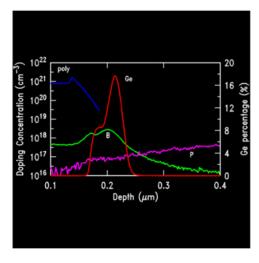
Having noise equations allows us to identify dominant

performance limits, is it &. Azi(57) or \$6 ???

Optimum Digital Ge Profiles

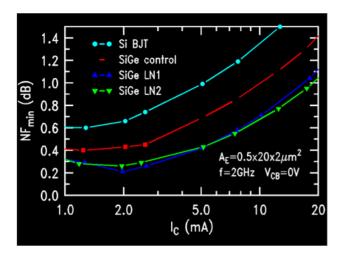
- . More Ge in the base is needed for higher beta
- . Ge edge must be pushed towards the surface





NF_{min} (2GHz) vs Profile

 $\bullet\,$ Higher beta and f_T are translated into lower RF noise



Conversion between representations

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Conversion Between Different noise formats.

 $= I_{n_1} - \frac{\Gamma_{i_1}}{\Gamma_{2i}} \cdot I_{n_2}$

Imput noise voltage and current. Chain representation,

Without thermal noise. In
$$\rightarrow$$
 22 IB $S_{In1} = 22 I_B$

$$\frac{I_{n1} I_n x^* = 0}{Y_{n2}} \qquad I_{n2} \rightarrow \qquad 22 I_C \qquad S_{In2} = 28 I_C$$

$$V_{na} = -\frac{I_{n2}}{Y_{21}} \qquad S_{vn} = \frac{V_{n4} V_{n4}}{S_f} = \frac{S_{ic}}{|Y_{21}|^2}$$

$$I_{na} = I_{n1} + I_{11} \cdot V_{n4} \qquad S_{in} = \frac{I_{n4} I_{n4}}{S_f} = \frac{S_{In2}}{|I_{n4}|^2}$$

$$I_{n1} = I_{n2} - \frac{I_{11}}{Y_{21}} \cdot I_{n2}$$

$$I_{n2} = I_{n3} - \frac{I_{14}}{I_{n4}} \cdot I_{n2}$$

$$I_{n3} = I_{n4} - \frac{I_{n4}}{I_{n4}} \cdot I_{n4}$$

$$I_{n4} = I_{n4} - \frac{I_{n4}}{I_{n4}} \cdot I_{n4}$$

$$I_{n5} = I_{n6} - \frac{I_{n6}}{I_{n6}} \cdot I_{n6}$$

$$I_{n6} = I_{n6} - \frac{I_{n6}}{I_{n6}} \cdot I_{n6}$$

$$I_{n7} = I_{n7} - \frac{I_{n7}}{I_{n7}} \cdot I_{n7}$$

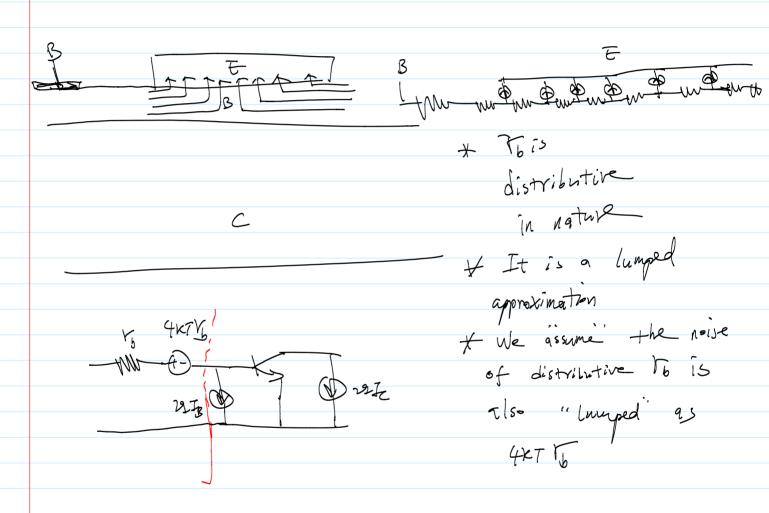
$$I_{n8} = I_{n8} - \frac{I_{n8}}{I_{n8}} \cdot I_{n8}$$

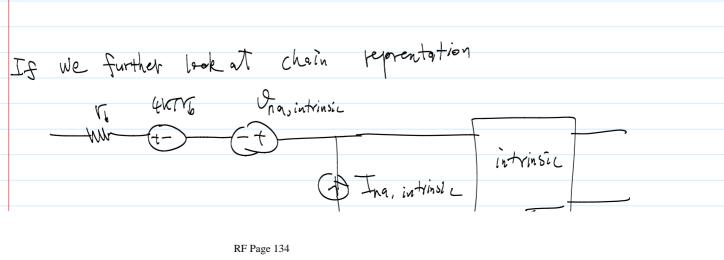
$$= I_{n_1} - \frac{I_{n_2}}{h_{n_1}}$$

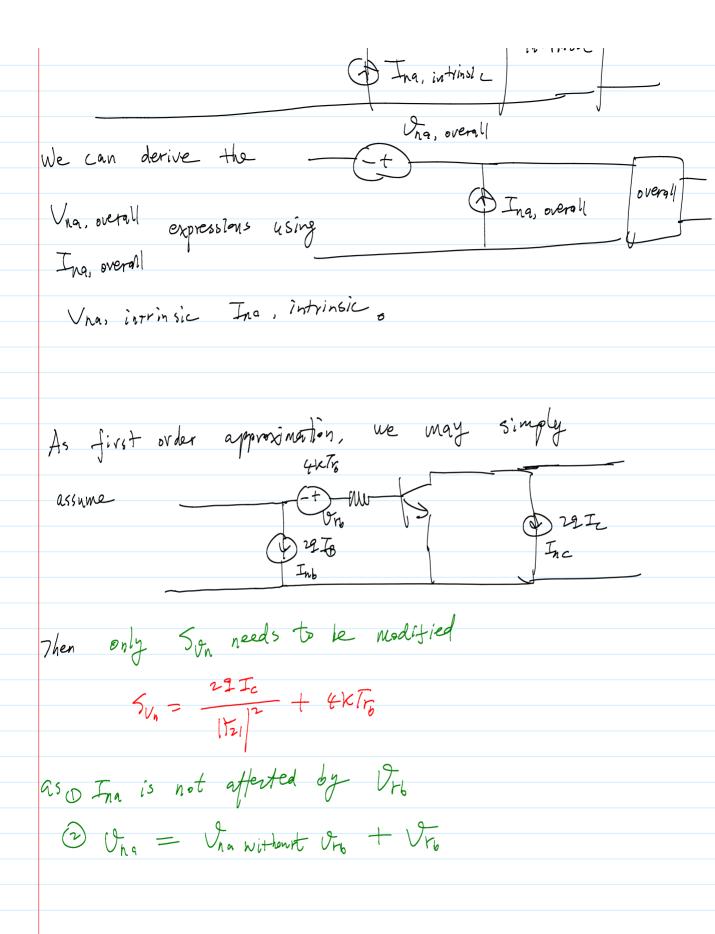
$$V_{n_1 in}^{\dagger} = 29 I_{c} \cdot \frac{I_{n_1}^{\dagger}}{|I_{n_1}|^2}$$

$$H_{n_1} = \frac{Y_{n_1}}{Y_{n_1}}$$

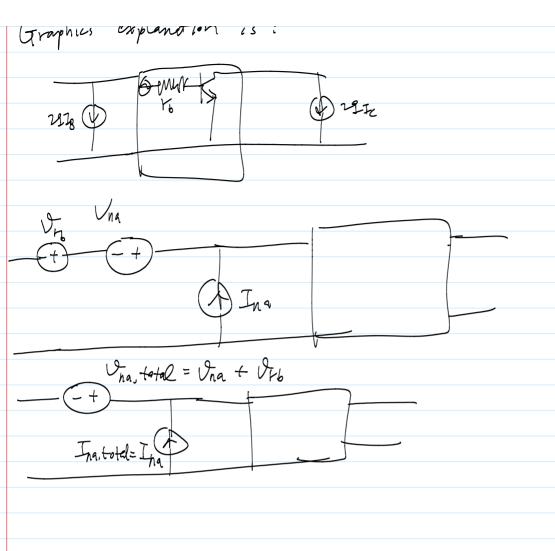
$$S_{in} V_{n_1}^{\dagger} = \left[S_{v_n i_n}^{\dagger}\right]^{\dagger} = 2 I_{c} \cdot \frac{I_{n_1}}{|I_{n_1}|^2}$$







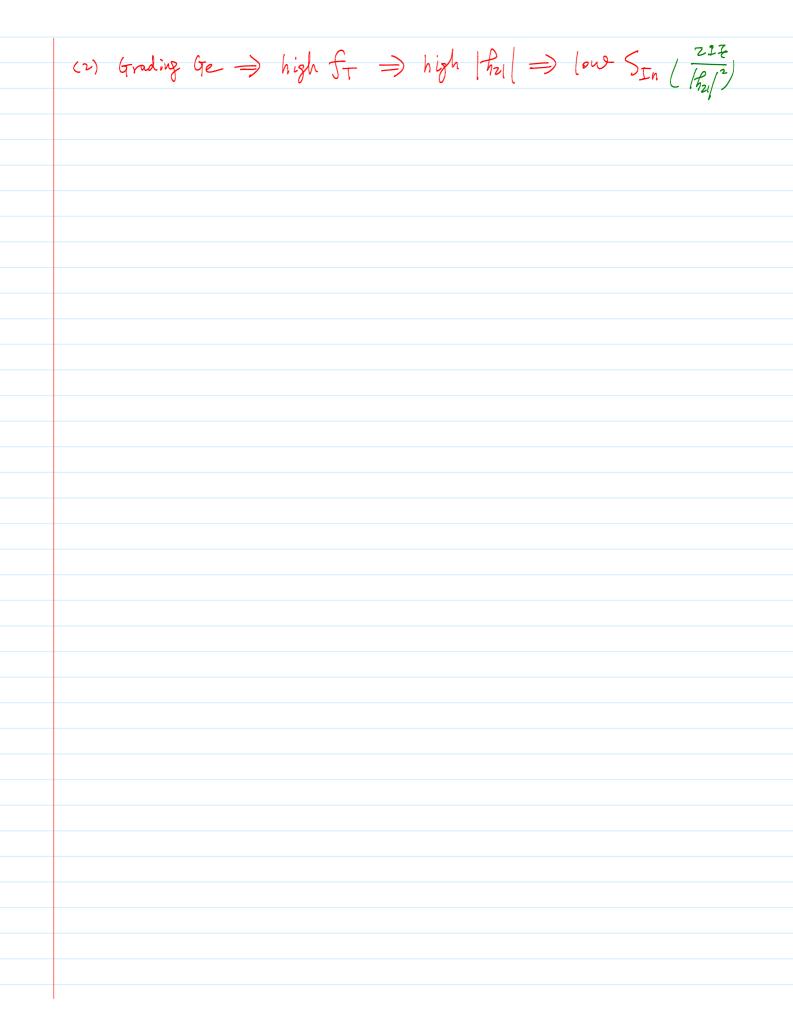
Graphics explanation is:



Summary of Sun San Sanut in site HBTs

$$S_{VN} = 4kTV_0 + \frac{29T_c}{|Y_1|^2} \qquad |Y_4| \approx 9m \approx \frac{T_c}{4k}$$

$$S_{In} = 29T_8 + \frac{21T_c}{|Y_4|^2} \qquad |H_{11}| \times f \approx f_T \quad |H_{11}| \times f_T \quad |H_{$$

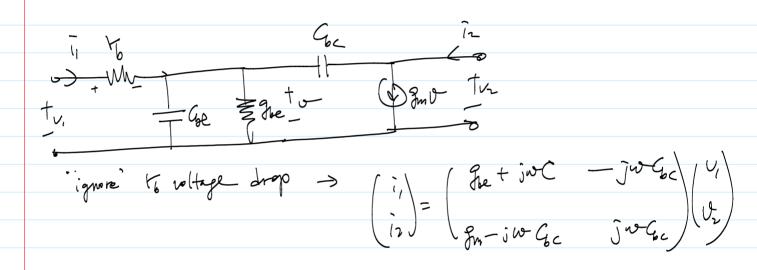


Transistor noise parameters expressions

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Analytical models for noise parameters

- 1) express y-parameters using gm, beta, C, fT variables one can associate with biasing, sizing, and device design (such as fT)
- 2) Calculate Svn, Sin and Sinvn*
- 3) Calculate noise parameters



$$Y_{1} = \frac{g_{m}}{\beta} + j_{w}C_{i}$$

$$C_{i} = G_{be} + G_{c}$$

$$Y_{12} = -j_{w}G_{c}$$

$$G_{e} = g_{m}T_{g} + C_{t}e$$

$$Y_{11} \approx g_{m}$$

$$g_{m} \approx \frac{T_{c}}{4} \quad \text{or replace } T_{c}$$

$$Y_{22} = j_{w}G_{c}$$

$$with g_{m} \cdot U_{t}$$

Nove we can express Sin Sun Staut using

familiar variables such as Jm. B. Tf. Ge. etc.

The form of the state of the state of the sun of the state of the sun of the state of

Ts.opt =
$$\sqrt{\frac{5in}{5vn}} - \left[\frac{Im(S_{in}v_n^*)}{5v_n}\right]^2$$
 derive it yourself

$$= \sqrt{\frac{3m}{2kn}} + \frac{1}{k} + \frac{voc_i^2}{2g_nk_n} \left(1 - \frac{1}{2g_nk_n}\right)$$

$$B_{s,opt} = -\frac{I_m(S_m V_n^*)}{S_{s,opt}} = -\frac{\omega C_{\bar{i}}}{2 J_m R_n}$$

derivation example:

$$5v_n$$

$$S_{i_1v_1t} = \frac{2gI_c}{\left|\frac{I_c}{V_t}\right|^2} \cdot \left(g_{e} + jwC_i\right)$$

$$\frac{5i_{1}v_{1}^{*}}{\left|\frac{I_{c}}{V_{t}}\right|^{2}} \cdot \left(\frac{g_{1}e}{V_{t}} + j_{w}C_{i}\right)$$

$$\frac{\left|\frac{I_{c}}{V_{t}}\right|^{2}}{\left|\frac{I_{c}}{V_{t}}\right|^{2}} \cdot \frac{2I_{c}\left(kT\right)^{2}}{I_{c}} = wC_{i}\frac{2\cdot\left(kT\right)^{2}}{I_{c}}$$

$$\frac{I_{m}\left(S_{in}V_{n}^{*}\right)}{I_{c}} = \frac{vC_{i}}{I_{c}}\frac{2\cdot\left(kT\right)^{2}}{I_{c}}$$

$$S_{vn} = 4kTR_{n}$$

$$B_{opt} = -\frac{\omega C_{i} \cdot \frac{2}{I_{c}} \cdot \frac{2}{2}}{4kTR_{n}} = -\omega C_{i} \cdot \frac{1}{2R_{n}} \cdot \frac{1}{I_{c}} \cdot \frac{kr}{2}$$

$$= -\omega C_{i} \cdot \frac{1}{2mR_{n}}$$

Bs, opt <0. Inductive source needed to noise noth ineginary part

$$F_{min} = 1 + \frac{1}{B} + \sqrt{\frac{2 f_m R_n}{B}} + \frac{2 R_n (w C_i)^2}{g_m} (1 - \frac{1}{2 g_m R_n})$$

* high B

* low to are needed for low NFmin

* high ft

Sizing for noise match

Thursday, September 06, 2012

device sizing.

increasing emitter length (EL)

Zsopt = Ts.apt & EL

(why?)

just like to & - .

2) for the same VBZ, NFmin is independent of EL

Just like ft. it is a property of the technology

Noise matching

a scale device size such that

Rs, opt = Rs

2) choose L for

w-L = Xopt.

Zs, opt = Rs, opt + j Xs, opt = +

noise matching + impedance matching

with certain approximation (see text)

under various assuptions, =)

Simultaneous noise and impedance match

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Can we possibly achieve noise matching and impedance matching at the same time without increasing noise figure? - Yes.

Now consider adding LE - emitter inductor Whe new two port device + LE NFmin \approx NFmin RS, opt \approx Rs, opt Levia through linear circult analysis => Rn = Rn device

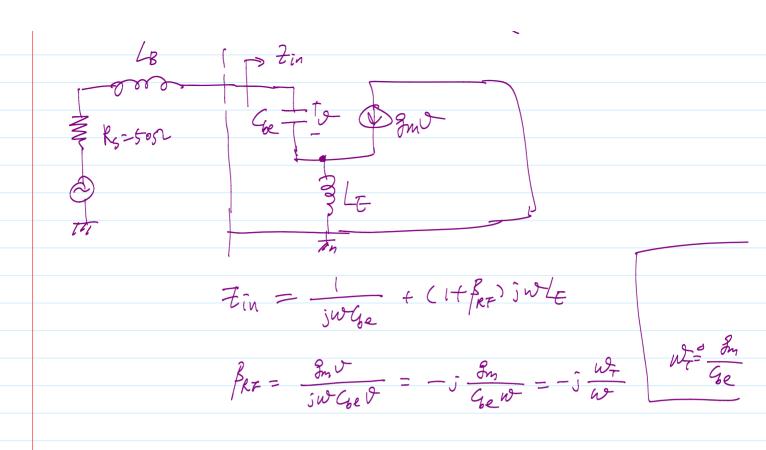
Courb

Sopt = Xsopt -LE can be chosen to produce peal part Zin RelZin) = WT.LE = Rs

So the real part is impedante matched (Z-match)

Luckily. The Xs, apt is also the (Xin) X So

LB [> Zin



Thus:
$$Zin = \frac{1}{j\omega Ge} + j\omega L_{\xi} + \omega T_{\xi}$$
 $L_{\xi} = \frac{R_{\xi}}{2\lambda f_{\tau}}$
 $L_{\xi} = \frac{R_{\xi}}{2\lambda f_{\tau}}$
 $U_{\tau}L_{\xi} = R_{\xi}$
 $V_{\tau}L_{\xi} = R_{\xi}$

* Even if these assumptions are not always valid.

We can tolerate some noise mis-moth as long as

it is not too far off and Rn is small

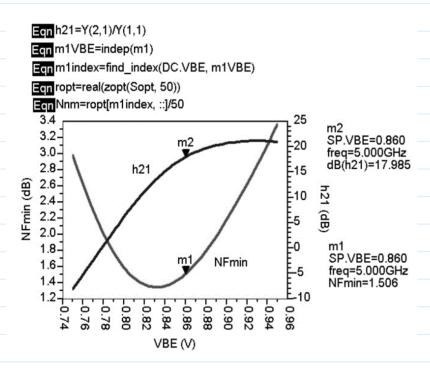
* The insight can still be used at least to

noise moth the real part, + inpedance mothing.

* For requirement determines To needed. Let fixed they

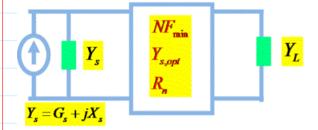
Rs (500) then determines El needed.

biasing I sizing example



$$NF = NF_{\min} + \frac{R_n}{G_s} |Y_s - Y_{s,opt}|^2$$

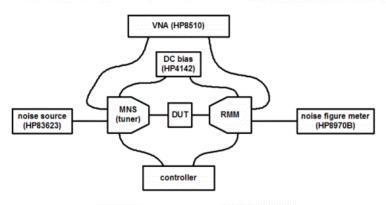
- NF is determined by noise parameters + source
- NF => NFmin when Ys = Ys,opt (noise matching)
- Rn determines sensitivity to deviation from Ys,opt



All of the noise parameters are important!

Noise Parameter Measurement Setup

ATN-NP5 system: solid-state source tuner Measure both ac and noise parameters)



ATN-NP5 noise measurement system setup

http://sdrv.ms/PGtOun