ELEC 5260/6260 – Cache and Virtual Memory and CPUs (Chapter 3)

1. From the end of Chapter 3 of the text book, do the following problems:
   Q3.26 (types of cache misses)
   Q3.27 (average memory access time)
   Q3.28 (cache hit rate)
   Q3.30 (cache patterns)
   Q3.31 (page address translation)
   Q3.36 (ARM pipeline)
   Q3.37 (ARM pipeline)

2. Do some research to find out what main processor is used in either the Nintendo Wii video game console or in the Apple iPhone 6. For the selected processor, look up and report the following characteristics:
   a. Cache memories:
      i. Number of "levels" (ex. Level 1, Level 2, etc).
      ii. Separate instruction and data caches or one unified cache for both
      iii. Cache capacity for each cache level
      iv. Degree of associativity of each cache: direct-mapped or value of N if N-way set associative
      v. Cache format: number of lines, number of bytes per line
      vi. Write strategy (write-through, write-back).
   b. Virtual memory support:
      i. Is a memory management unit (MMU) used?
      ii. What is the capacity of the virtual address space?
      iii. Is paging and/or segmentation used?
      iv. What are the page and/or segment sizes?
      v. Does the MMU use a single or multiple page/segment tables?