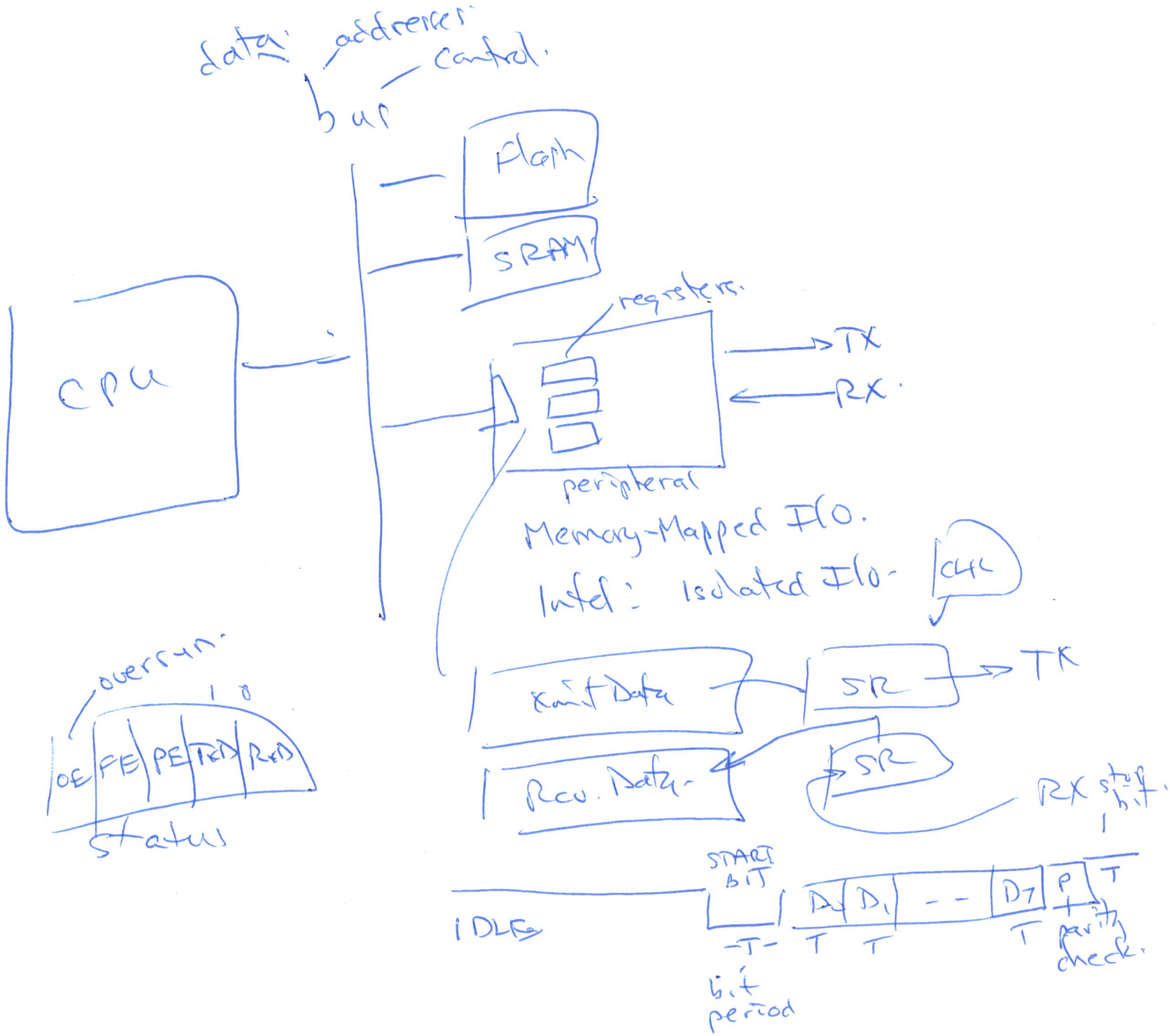
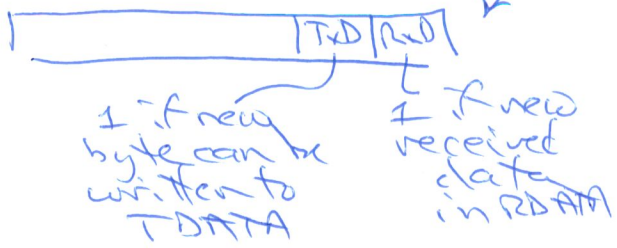

data
address
control
bus
Flash
SRAM
CPU
registers
TX
RX
peripheral
Memory-Mapped I/O
Intel: Isolated I/O
CLK
overrun
OE
FE
PE
TRDY
RRDY
status
Xmit Data
SR
TX
Rcv. Data
SR
RX
stop bit
IDLE
START BIT
D0
D1
D7
P
parity check
T
bit period

Accessing the UART with subroutines

Define symbolic labels for UART register addresses.

```
RDATA   EQU  0x40000000   ; Received data reg
TDATA   EQU  0x40000004   ; Xmit   "    "
STATUS  EQU  0x40000008   ; UART status
```




```
; Get_Data - return next received
; data byte in R0
;
Get_Data  LDR  R0,=STATUS
Wait1     LDRB R1,[R0]      ; Get status byte
          TST  R1,#0x01     ; check RxD bit
          BEQ  Wait1        ; Repeat until RxD=1 (new byte received)
          LDRB R0,[R0,#-9]  ; Read RDATA byte
          BX   LR           ; return
```

```
; Send_Data - send byte passed in R0
;
Send_Data LDR  R1,=STATUS
Wait2     LDRB R2,[R1]      ; Get status byte
          TST  R2,#0x02     ; Check TxD bit
          BEQ  Wait         ; Repeat until TxD=1 (TDATA ready for new byte)
          STRB R0,[R1,#-4]  ; write byte to TDATA
          BX   LR           ; return
```