Inter-IC Sound (I²S) Bus

- Optimized for digital audio data transmission
- 3-line serial bus lines
  - **SD**: Two time-multiplexed data channels
  - **WS**: Word Select (0 = left channel, 1 = right channel)
  - **SCK**: Clock
    - Bus master generates SCK and WS
    - Bus master = transmitter or separate controller
    - SCK synchronizes transmitter and receiver
- Serial data format
  - Two’s complement, MSB sent first
  - If system word > #transmitted bits, truncate after LSB
  - If system word < #transmitted bits, add 0’s after LSB

Philips I²S Specification:
http://www.classic.nxp.com/acrobat_download2/various/I2SBUS.pdf
I²S system configuration and timing

Source: Philips Semiconductor I²S bus specification
STM32 SPI/I²S Module

- Four supported I²S protocols:
  - I²S Phillips standard.
  - MSB-justified standard (left-justified),
  - LSB-justified standard (right-justified),
  - PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)

- Data formats of 16-bit, 24-bit or 32-bit
- Packet frame is 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit, 32-bit data frame)
- Data direction is MSB first
- 16-bit register for transmission/reception with one data register for both channel sides
- DMA capability for transmission and reception (16-bit wide)
- Half or full duplex communication
- Master or slave operations
STM32 SPI/I²S Module

- 8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8 kHz to 192 kHz)
- Master clock may be output to drive an external audio component. Ratio is fixed at $256 \times \text{FS}$ (where FS is the audio sampling frequency)
- Both I2S (I2S2 and I2S3) have a dedicated PLL (PLLI2S) to generate an even more accurate clock.
- I2S (I2S2 and I2S3) clock can be derived from an external clock mapped on the I2S_CKIN pin.
- Programmable clock polarity (steady state)
- Underrun flag in slave transmission mode, overrun flag in reception mode (master and slave), and Frame Error flag in reception and transmission mode (slave only)
STM32F4xx
I²S function
(Pins shared with SPI)
STM32F4xx I²S registers

**SPI_I2SCFGR**

- **I2SMOD**: 0 = SPI mode, 1 = I2S mode
- **I2SE**: 1 = enable I²S
- **I2SCFG**: 00 = slave xmit, 01 = slave rcv, 10 = master xmit, 11 = master rcv
- **PCMSYNC**: used in PCM mode
- **I2SSTD**: I²S Standard: 00 = Philips, 01 = MSB justified, 10 = LSB justified, 11 = PCM
- **CKPOL**: steady-state clock level (0/1)
- **DATLEN**: data length: 00 = 16-bit, 01 = 24-bit, 10 = 32-bit
  (16-bit data register => 2 reads for 24/32-bit data)
- **CHLEN**: word frame length: 0 = 16-bit, 1 = 32-bit
  - LSBs = 0 for 16/24-bit data in 32-bit frame

Must set this bit to select SPI or I²S
I²S Philips protocol  \((\text{CPOL} = 0)\)

- WS latched on falling edge of CK
- Xmit: latch data on falling edge of CK
- Rcv: read on rising edge of CK
I²S MSB justified standard

WS generated with first data bit (MSB)

16/32 data in 16/32 frame

24 data in 32 frame
I²S LSB justified standard

16/32 data in 16/32 frame

24 data in 32 frame
I²S PCM standard

- No channel-side information
- Short and long frame formats (configure with PCMSYNC bit)
  - Long frame: WS asserted for 13 bits
  - Short frame: WS asserted for 1 bit
I²S clock generator

- Fs = audio sample frequency
- I²S bitrate = (#bits/channel) x (#channels) x Fs
  - Ex: 16-bit stereo (2 channels)
    - I²S bitrate = 16 x 2 x Fs

Fs: Audio sampling frequency
I2S clock generator

- I2SxCLK source = PLLI2S output or ext. input (I2S_CKIN)
- Fs = 48kHz, 96kHz or 192kHz
- Fs = I2SxCLK / [(CF*2) * (2*I2SDIV+ODD)*8]
  CF = channel frame (16 or 32 bits)