1. From the end of Chapter 4 of the text book, do the following problems:
   Q4.10 (bus timing for a write operation with wait states)
   Q4.12 (UML state diagram for a burst read with wait states)
   Q4.15 (timing diagram of a DMA operation)
   Q4.18 (UML sequence diagram for a DMA operation)

2. Design an external memory subsystem for an STM32F407-based embedded system. The memory is to have the following characteristics.
   a. 64 Mbytes of static RAM. Use the Internet or library to find commercial memory chips for this design. Use as few memory chips as possible.
   b. You may select any address range and timing characteristics (speeds) for the memory, but they must be compatible with the STM32F407 Flexible Static Memory Controller (FSMC) – Chapter 36 of the STM32F4xx Reference Manual.
   c. List the address range of each memory device, and the values to be written to the STM32F407 FSMC registers to enable your external SRAM design to be used.
   d. Look up and report the access time(s) for the memory device, and determine the number of required CPU clock cycles necessary for a read cycle.
   e. Sketch the memory subsystem, showing the interconnections between the memory devices and STM32F407, including any additional logic circuitry. Provide sufficient detail to show all connections. Use the format of the flash and SRAM pages of the uCdragon board schematics from the class presentation.