ELEC 5260/6260 –Bus timing and memory systems (Chapter 4)

1. From the end of Chapter 4 of the text book, do the following problems:
   Q4.9 (bus timing for a read operation with wait states)
   Q4.11 (bus timing for a burst write operation)
   Q4.12 (two UML state diagrams for a burst read with wait states)
   Q4.15 (timing diagram of a DMA operation)
   Q4.22 (UML sequence diagram for an SDRAM read with refresh)

2. Design an external memory subsystem for an STM32L476G-based embedded system. The memory is to have the following characteristics.
   a. 32 Mbytes of static RAM. Use the Internet to find commercial memory chips for this design. ***Use as few memory chips as possible.***
   b. You may select any address range and timing characteristics (speeds) for the memory, but they must be compatible with the STM32L476G Flexible Static Memory Controller (FSMC). *(Reference: Chapter 16 of the STM32L4x6 Reference Manual.)*
   c. List the address range of each memory device, and the values to be written to the STM32L476G FSMC registers to enable your external SRAM design to be used.
   d. Look up and report the access time(s) for the memory device, and determine the number of required CPU clock cycles necessary for a read cycle, assuming the maximum CPU clock speed of 80MHz.
   e. Sketch the memory subsystem, showing the interconnections between the memory devices and STM32L476G, including any additional logic circuitry. Provide sufficient detail to show all connections. Use the format of the uCdragon board flash and SRAM schematics in the class presentation.

3. Look up and describe the characteristics of the Flash memory integrated circuit chip on the STM32L476G-Discovery board, and how this device is interfaced to the STM32L476G microcontroller.