

ELEC 5260/6260 – Homework #9
Bus timing and memory systems (Chapter 4)

Due: Monday, March 9, 2010

1. From the end of Chapter 4 of the text book, do the following problems:
 - Q4.4 (bus timing for a write operation with wait states)
 - Q4.7 (UML state diagram for a burst read with wait states)
 - Q4.10 (timing diagram of a DMA operation)
 - Q4.13 (UML sequence diagram for a DMA operation)

2. Look up and report the characteristics of the cache memories in the ARM Cortex-A8 processor, which is used in a number of the current smart phones and other multimedia devices. You should list the cache capacity, cache format (number of lines, number of bytes per line), degree of associativity (direct-mapped or value of N if N-way set associative), write strategy (write-through, write-back).

3. Design of an external memory subsystem for an LPC2292-based embedded system. The memory is to have the following characteristics.
 - a. 16 MByte flash memory and 2 MByte static RAM. Use the Internet or library to find commercial chips to use for the memory, *other than the chips on the uCdragon boards.*(You should be able to use one chip of each type.)
 - b. You may select the address range for each memory and timing characteristics (speeds), but they must be compatible with the LPC2292 external memory interface and controller.
 - c. List the address range of each memory, and the values to be written to the LPC2292 external memory controller registers to enable your flash and SRAM design to be used.
 - d. Sketch the memory subsystem, showing the interconnections between the memory devices and LPC2292, including any additional logic circuitry. Use the format of the flash and SRAM pages of the uCdragon board schematics posted on the course web page.