ASIC Physical Design
Top-Level Chip Layout

References:

• M. Smith, *Application Specific Integrated Circuits*, Chap. 16
• Cadence Virtuoso User Manual
Top-level IC design process

- Typically done **before** individual circuit block layouts
  - Top-level netlists usually created before any layout
- Create top-level schematic
  - "Components" are functional blocks and I/O pads
  - Blocks include IP and user-created modules
- Create a chip "floor plan" from the schematic
  - Place functional blocks and I/O pads
  - Connections shown as overflows
- Route top-level connections (automatic or interactive)
- Eliminate overflows, DRC errors, shorts
- Create layouts of user-designed modules
Chip floorplan

standard-cell area

fixed blocks

I/O pads

0.02 in 500 μm
Modulo-7 counter in pad frame
MOSIS SCMOS Pad Library

- Includes 6 pad types:
  - Input & output pads with buffers
  - VDD & GND pads with ESD
  - Analog IO pad with ESD
  - Analog reference pad with ESD
- Assemble into a “frame” in which pads butt against each other
  - Allows VDD & GND wires to form a continuous ring
  - Special “spacer” and “corner” pads complete the ring
- ADK tools will generate a pad frame from a schematic
MOSIS
TSMC 0.35um
Hi-ESD
Pad Frame

(1) lambda=0.30um
MOSIS
TSMC 0.35um
Hi-ESD
Pad Frame

Physical layout

Corner pad (passes VDD/GND)

VDD/GND wires form continuous ring through the pad frame

Spacer pad if no signal
MOSIS I/O Pad Schematic

- Bonding Pad
- Inputs to logic ckts
- Output enable
- Outputs from logic ckts
Simplified pad circuit

\[
\begin{align*}
\text{ENABLE} &= 0 \quad (\text{ENABLE\_bar} = 1) \\
\varphi_2 &\text{ off} \\
\varphi_4 &\text{ on} \quad \rightarrow \text{pulls 0 to VDD} \Rightarrow \varphi_7 \text{ off} \\
\varphi_5 &\text{ off} \quad \rightarrow \text{pulls 0 to GND} \Rightarrow \varphi_6 \text{ off} \\
\end{align*}
\]

\[
\begin{align*}
\text{ENABLE} &= 1 \\
\varphi_3 &\text{ on} \quad \overline{\varphi_3} = \overline{\text{out}} \Rightarrow \text{Inverted by } \varphi_7/\varphi_8 \\
\varphi_4 &\text{ off} \\
\varphi_5 &\text{ on} \\
\varphi_6 &\text{ off}
\end{align*}
\]
ADK I/O Pad Schematic

(Configured as output pad)
MOSIS 1.6 μm bidirectional pad

Source: Weste, “CMOS VLSI Design”
ASIC frame + core in Virtuoso
Top-level bottom-up design process

- Generate block layouts and for each block:
  - Import the GDSII stream into a Virtuoso library
  - Import the Verilog netlist into the library
  - Perform DRC and LVS on each block until “clean”
  - Create a schematic symbol from the netlist in the library
- Create a block diagram/schematic in Virtuoso “Composer”
  - Create a top-level block library and create a schematic view
  - Instantiate schematic symbols from the library
  - Interconnect with nets and add pins
  - Check and save
- Create a layout from the schematic diagram
Top-level block schematic in “Composer”

Figure 12.1: Starting schematic showing the three connected modules
Before module and I/O placement

Blocks initially outside boundary

Figure 12.3: Initial layout before module and I/O placement
After placing modules
Power routing between blocks
Nets shown as “overflows”
Routed circuit block
Block symbol (to connect to I/O pads)

Figure 12.11: Symbol for the Three Blocks example core
Pad frame with signal wires
Zoomed view of pad frame

Figure 12.13: Pad frame with signal wires (zoomed view)
Schematic: block + pad frame

Figure 12.14: Frame and core components connected together
Placement of frame and core
Power/ground routed manually
Before signal routing
After routing – final layout
Floorplanning (Text chap. 15, 16)

- **Floorplanning**: arrange major blocks prior to detailed layout to optimize chip area
  - input is a netlist of circuit blocks (hierarchical)
    - after system “partitioning” into multiple ICs
  - estimate layout areas, shapes, etc.
    - Flexible blocks – shape can be changed
    - Fixed block – shape/size fixed
- do initial placement of blocks (keep highly-connected blocks close)
- decide location of I/O pads, power, clock
Floorplan a cell-based IC (Fig. 16.6)
- may have to fit into “die cavity” in a package

Initial random floorplan

Blocks moved to improve floorplan

Reduced congestion after changes

Heavy congestion below B

flexible standard-cell blocks (not yet placed)

flexible standard-cell blocks (with estimated placement)
Congestion analysis (Fig. 16.7)

Initial 2:1.5 die aspect ratio

Altered to 1:1 aspect ratio

A & B resized to reduce congestion
Routing a T junction

1. Adjust channel A first.

   - Block 1
   - Block 2
   - Block 3

   - Channel B
   - Block pin
   - T-pin

   2. Now we can adjust channel B.

   Preferred

2. Adjust channel B first.

   - Block 1
   - Block 2
   - Block 3

   - Channel B
   - Block pin

   2. Now we cannot adjust channel A.

   Constraining
Define channel routing order

• Make “cuts” (slice in two) to separate blocks
• Slicing tree, corresponding to sequence of cuts, determines routing order for channels
  - route in inverse order of cuts
Non-slicing structure

Cyclic constraint prevents channel routing

Cannot find slicing floorplan without increasing chip area

Slicing floorplan possible, but inefficient in use of chip area
Power distribution

Uses special power pads, wires, routing

Option a:
m1 for VSS
m2 for VDD
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Potential problems in routing channel

Many layer changes/vias if VDD/VSS on different layers

Option b:
m1 parallel to longest side
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Easier routing but more vias

Array of via contacts for VDD/VSS Buses.
Clock distribution (minimize skew)

Often use “clock tree” structure