

## **ELEC 5250\_6250 Project 9**

### **Due: 11 am on Friday, November 4, 2011**

ELEC 5250 Students: Do this assignment with the modulo-6 counter circuit.

ELEC 6250 Students: Do this assignment with the divider circuit.

Again, for this assignment, a project report is to be submitted electronically as a Word or PDF document.

You are to create a layout of a “tiny chip” that instantiates one of the standard cell blocks designed in the previous assignment, plus pads for signal and power/ground.

ELEC 5250 students – use two VDD and two GND pins, in addition to your input and output signals.

ELEC 6250 students - Since the tiny chip is limited to 40 pins, use the same 8 inputs as both the divisor and half of the dividend. Use multiple VDD and GND pins, so that all 40 pins have connections.

1. If you have not already done so, generate a symbol for your divider or counter, ensuring that you add the physical component property to associated the symbol with the layout cell created previously. Insert a screen capture of the symbol into your report.
2. Design a top-level schematic of the chip in Design Architect-IC. Insert a screen capture of the schematic in your report.
3. Design the chip layout in IC Station, ensuring that your power/ground wires are appropriately sized. Insert a screen capture of the chip layout in your report.
4. Perform a design rule check (DRC) and a layout-vs-schematic (LVS) check on the chip. Insert screen captures into your report, showing that both DRC and LVS checks passed. Note that pads should be excluded from the DRC.