

ELEC 5250_6250 Project 8

Due: Thursday, October 27, 2011

ELEC 5250 Students: Do this assignment with the modulo-6 counter circuit.

ELEC 6250 Students: First practice with the modulo-6 counter (do not submit), and then do the assignment with the divider circuit.

For this assignment, a project report is to be submitted electronically as a Word or PDF document.

1. If necessary, use LeonardoSpectrum to resynthesize your circuit(s) in the TSMC 0.35um technology. You will need only the Verilog netlist to proceed with physical design.
2. Import the Verilog netlist of your circuit into Design Architect-IC. Use the netlist generated by Leonardo (which used the standard cells in the ADK library.) Put a “screen capture” of the schematic diagram, from Design Architect-IC, into your project report.
3. Generate the design viewpoints needed for IC Station and Calibre (use the adk_dve script).
4. Create a layout of your circuit in IC Station, using the automated place and route features of the tool.
5. Run the design rule checker (ICrules) and correct any design rule violations. Put a screen capture of the final layout into the report, showing “0 violations” in the status area of the screen.
6. Make the following three changes to the layout, ensuring that no design rules are violated in the process. If one of these changes was done in correcting a design rule violation, you do not need to do additional changes of that type.
 - a. Move one wire segment.
 - b. Add a metal “shape” to a wire.
 - c. Make one wire segment wider.

For each of these changes, insert a screen capture into your project report, showing the change.

7. Use Calibre to run a Layout vs Schematic (LVS) check. Cut and paste the information (one page) from the LVS report showing no errors into your project report.
8. Use Calibre to run a parameter extraction (PEX). In your project report, copy the first page of the original SPICE-level netlist, created by Design Architect-IC, and the first page of the extracted netlist into your project report. Also, from the extracted netlist, copy a portion of the design showing extracted parasitic capacitances.
9. Read each of the report files created by IC Station. For each of these, write a sentence in your project report, noting one “interesting” thing you noticed in the IC Station report.

The next assignment will require simulation of the extracted netlist from step 8 above.