

ELEC 5250_6250 Project 7 (Option #1)

Due: Tuesday, October 18, 2011

The objectives of this exercise are twofold. First, we want to develop a script to control the synthesis process. Second, we want to compare the results produced by the two synthesis tools: LeonardoSpectrum and Synopsys Design Compiler.

1. Design a script file for Synopsys Design Compiler that will generate a Verilog netlist and SDF file of your divider circuit, plus a report of path delays and area.
2. Compare the synthesized design to that produced by LeonardoSpectrum, noting differences in area and delay.
3. Simulate the synthesized circuit, with SDF file, using your previous test bench or “do file”, and compare the simulation results with those obtained with the Leonardo-synthesized circuit.

Note the following:

- a. The script and setup files that I used for the class example are posted on the class web site, next to the lecture slides for that day.
- b. The Synopsys Design Compiler needs to be run on a Linux machine. Before you can use the Synopsys tools, enter the command “synthesis” to run a script that we’ve created to set up the appropriate paths and environment variables for Synopsys.
- c. After running the above script, you may invoke either the command shell (dc_shell) or the GUI (design_vision) to run your script. The GUI is handy for examining the synthesized circuit in schematic form, and browsing through the various design elements and reports.

To be submitted:

1. A printout of your synthesis script file.
2. A summary of the synthesized circuit (number of cells and area) for the LeonardoSpectrum and Synopsys synthesized circuits.
3. A summary of the worst-case paths, and max clock frequency, for the LeonardoSpectrum and Synopsys synthesized circuits.
4. A short discussion of the main differences (area and speed) between the two synthesized designs.
5. Two pages of the simulation listing window, showing the operation of the synthesized circuit, including delays.