

ELEC 5250/6250 – Homework Project 3

Part 1 Due Tuesday, September 6

Part 2 Due Thursday, September 8

You are to perform four simulations of the modulo-6 counter designed previously. Your tests should be designed to fully verify the functionality of the counter, as discussed in class.

Part 1:

1. Simulate the behavioral model, using a “do file” (command file).
2. Simulate the structural model, using the same “do file”.

Part 2:

1. Simulate the behavioral model, using a testbench.
2. Simulate the structural model, using the same testbench.

For each, generate a printout of a “wave” window from Modelsim, and hand-annotate to show me where in the simulation each of the counter’s functions is being verified (clearing, counting, loading). You need to convince me that all functions have been verified in the simulation.

Items to submit:

1. Your original schematic from Project 1.
2. Your behavioral and structural VHDL models from Project 2, corrected as necessary.
3. Part 1: A printout of your “do file”.
Part 2: A printout of your testbench.
4. A printout of the four annotated wave windows.