The MOSIS Service

Hi-ESD Pad Library

TSMC CMOS (0.35µ) Process

June 1999
TANNER CES GENERAL TERMS & CONDITIONS

Liability
All designs will be implemented under the Client's front-end specification. Our contracted engineering services are accomplished for the Client on a best effort basis. Quality assurance is achieved by arriving at a common understanding of the nature of the Project among the engineers and managers at the Client operation and at Tanner CES. Tanner Research is not liable for the functionality, quality, or performance of the Client's future Projects using components produced as part of the contracted work. Tanner Research is not liable if the Client chooses to use our recommended design or application methodologies. If prototype chips are delivered, the process vendors do not generally guarantee yield, quality, or performance of their products. Neither does Tanner Research extend any warranty to the contracted design and its fabricated results.

Non-Disclosure Agreement
Non-disclosure agreements (NDAs) serve the following purposes.

- Signed between the Client and Tanner Research, the NDA protects Client's original concept, status, and intentions in current and future product development and manufacturing.
- Signed between the Client and Tanner Research, the NDA protects Tanner Research' specific technologies, IC libraries, building blocks and methodologies that are developed prior to the Client Project, or developed specifically for the Client application.
- Specific non-disclosure or non-distribution conditions may be added to the Statement of Work for individual Client Projects. These conditions do not replace or supercede any previously signed NDA; rather they serve as additional constraints to the NDA.
- During or at the end of the Client Project, if we communicate with a process vendor or receive fabricated parts from a process vendor which will be forwarded to the Client, we assume that the Client is also a current customer of the vendor. We may request Client to provide a proof of its NDA with the vendor before any such communication or transaction.

Ownership of Work Results
The Client owns the delivered version and the fabricated version of the work results from a contracted Client Project. These results are subject to the following re-distribution conditions:

- The Client agrees to use the work results only in its own Projects or products, as developed by the Client and on the Client's own site.
- The Client will not distribute copies of the delivered data files and documents (such as design, libraries, process technology setups, design flows and methodologies, software utilities, etc.) to any third parties or to any other Client site, with the following two exceptions:
  - Exception 1: If applicable, results can be delivered to the Government Agency sponsoring the Client Project, if such delivery is negotiated as part of the Client Project. During contract negotiations, the Client shall inform Tanner Research about such a delivery and receive advance agreement from us for the contents to be disclosed.
  - Exception 2: If applicable, results can be incorporated into published academic research or presented for academic purposes. During contract negotiation, the Client shall inform Tanner Research about such a presentation and receive advanced agreement from us for the contents to be disclosed.
- Any other exceptions shall be specified in a written document signed by both the Client and Tanner Research.

Tanner Research does not own the original design and application concepts from the Client. We agree not to disclose the Client's proprietary design and applications information. However, we shall distinguish the following items that remain the property of Tanner Research:

- The methodology used through the development of the Client Project, or that we planned for Client to apply the Project’s results, are usually either common knowledge in the industry or specific methods invented by Tanner Research. Using or adopting these methodologies in the Client Project does not institute the Client’s ownership to these methodologies.
- Client does not own Tanner Research’s general-purpose building elements (such as cell libraries, building blocks, IO pad cells, etc.) that we utilize in a contracted Project. These building elements are Tanner Research’s current design resources that are widely used internally and/or distributed as commercial products. Using these building elements does not institute the Client’s ownership of them.

Protect Tanner Research’s Engineering Resources
Through the entire Client Project cycle, starting from bid and proposal to the end of the Project, the Client will contact various engineering resources within Tanner Research. These resources may include Tanner Research's employees and its associates (subcontracting firms or individuals). The Client agrees not to recruit or hire any of these individuals or contract with any firms during the three years following Project completion.
MOSIS TSMC/HP 0.35um Hi-ESD Minimum Pad Frame

(1) lambda = 0.20um

pitch = 0.09 mm
(450 lambda)

0.9 mm
(4500 lambda)

1.5 mm
(7500 lambda)

1.5 mm
(7500 lambda)
Hi-ESD Pad Dimensions

Hi-ESD Pad Dimensions

(1) \( \lambda = 0.20 \mu m \)

MOSIS TSMC/HP 0.35um

Hi-ESD Pad Dimensions

MOSIS TSMC/HP 0.35um

Hi-ESD Pad Dimensions

(1) \( \lambda = 0.20 \mu m \)
**Description:** Pad Library

Library: MOSIS TSMC 0.35P  Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples

Schematic: S-Edit  File: TannerLb\scmos\mTSMs035P.sdb
Module: Library

Mask layout: L-Edit  File: TannerLb\scmos\mTSMs035P.tdb
Cell: Lib_Pads

Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

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<th>Truth Table</th>
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<th>Drive</th>
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<td>N/A</td>
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</tbody>
</table>

Logic Equation

N/A

Delay Characteristics: N/A
This page is intentionally left blank.
**Pad Frame**

**Description:** Pad Frame

Library: MOSIS TSMC 0.35µm
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples

Schematic: S-Edit
File: TannerLb\scmos\mTSMs035P.sdb
Module: N/A

Mask layout: L-Edit
File: TannerLb\scmos\mTSMs035.tdb
Cell: FRAME

Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

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<td>1.5 mm</td>
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<td>2.25 mm²</td>
<td>N/A</td>
<td>N/A</td>
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**Logic Equation**

N/A

**Delay Characteristics:** N/A
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**Analog Ref Pad**

**Description:** Analog Reference Pad

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<th>Area</th>
<th>Equivalent Gate</th>
<th>Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 μ</td>
<td>90 μ</td>
<td>27000 μ^2</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Logic Equation**

N/A

**Delay Characteristics:** N/A
This page is intentionally left blank.
**Description:** Bi-Directional Pad with Buffer

**Library:** MOSIS TSMC 035P  
**Primitive Set:** Tanner SCMOS.Cells  
**Tanner.TIB.Samples**

**Schematic:** S-Edit  
**File:** TannerLb\scmos\mTSMs035P.sdb  
**Module:** PADBIDIR

**Mask layout:** L-Edit  
**File:** TannerLb\scmos\mTSMs035P.tdb  
**Cell:** PADBIDIR

**Mapping Macros:**  
GateSim: TannerLb\nettran\scmos\scms2sim.mac  
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

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<tr>
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<td>X</td>
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<td>X</td>
<td>In</td>
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<td>X</td>
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<td>0</td>
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</table>

**Height** | **Width** | **Area** | **Equivalent Gate** | **Drive**
---|---|---|---|---|
300 µ | 90 µ | 27000 µ² | N/A | N/A

**Logic Equation**

See truth table

**Delay Characteristics:** N/A
This page is intentionally left blank.
**Description:** Pad Frame Corner

Library: MOSIS TSMC 0.35µm
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples

Schematic: S-Edit
File: TannerLb/scmos/mTSMs035P.sdb
Module: N/A

Mask layout: L-Edit
File: TannerLb/scmos/mTSMs035P.tdb
Cell: PADFC

Mapping Macros: GateSim: TannerLb/nettran/scmos/scms2sim.mac
L-Edit/SPR: TannerLb/nettran/scmos/scms2tpr.mac

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<th>Width</th>
<th>Area</th>
<th>Equivalent Gate</th>
<th>Drive</th>
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<tbody>
<tr>
<td>300 µ</td>
<td>300 µ</td>
<td>90000 µ²</td>
<td>N/A</td>
<td>N/A</td>
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</tbody>
</table>

**Logic Equation**

N/A

**Delay Characteristics:** N/A
Ground Pad

**Description:** Ground Pad

Library: MOSIS TSMC 035P
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples

Schematic: S-Edit
File: TannerLb\scmos\mTSMs035P.sdb
Module: PADGND

Mask layout: L-Edit
File: TannerLb\scmos\mTSMs035P.tdb
Cell: PADGND

Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

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<th>Width</th>
<th>Area</th>
<th>Equivalent Gate</th>
<th>Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 μ</td>
<td>90 μ</td>
<td>27000 μ²</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Logic Equation:**

N/A

**Delay Characteristics:**

N/A
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Ground Pad Schematic PADGND

PadGnd

BONDING

Pad

TESDP W='175' L='34'
N=16
**Input Pad**

**PADINC**

**Description:** Buffered Input Pad with Complementary Signals

Library: MOSIS TSMC 035P  
Primitive Set: Tanner SCMOS.Cells  
Tanner.TIB.Samples

Schematic: S-Edit  
File: TannerLb\scmos\mTSMs035P.sdb

Module: PADINC

Mask layout: L-Edit  
File: TannerLb\scmos\mTSMs035P.tdb

Cell: PADINC

Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac

L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

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<th>Width</th>
<th>Area</th>
<th>Equivalent Gate</th>
<th>Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 µ</td>
<td>90 µ</td>
<td>27000 µ²</td>
<td>N/A</td>
<td>N/A</td>
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**Logic Equation**

See truth table

**Delay Characteristics:**

\[ T_{pd} = 0.28\text{ns} \]
\[ T_r = 0.24\text{ns} \]
\[ T_f = 0.18\text{ns} \]
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Input/Output Pad  

**Description:** Input/Output Pad

Library: MOSIS TSMC 035P  
Primitive Set: Tanner SCMOS.Cells  
Tanner.TIB.Samples

Schematic: S-Edit  
File: TannerLb/scmos/mTSMs035P.sdb

Module: PADIO

Mask layout: L-Edit  
File: TannerLb/scmos/mTSMs035P.tdb

Cell: PADIO

Mapping Macros: GateSim: TannerLb/nettran/scmos/scms2sim.mac
L-Edit/SPR: TannerLb/nettran/scmos/scms2tpr.mac

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<th>Width</th>
<th>Area</th>
<th>Equivalent Gate</th>
<th>Drive</th>
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</thead>
<tbody>
<tr>
<td>300 µ</td>
<td>90 µ</td>
<td>27000 µ²</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Logic Equation:**

N/A

**Delay Characteristics:**

N/A
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Input/Output Pad Schematic PADIO

mTSMs035P – MOSIS TSMC 0.35µm Hi-ESD Pad Cell Library

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**Padless Spacer**

**Description:** Padless Spacer without Bonding Pad

<table>
<thead>
<tr>
<th>Library: MOSIS TSMC 035P</th>
<th>Primitive Set: Tanner SCMOS.Cells</th>
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<tbody>
<tr>
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Schematic: S-Edit

- File: TannerLb\scmos\mTSMs035P.sdb
- Module: N/A

Mask layout: L-Edit

- File: TannerLb\scmos\mTSMs035P.tdb
- Cell: PADSPACE

Mapping Macros:

- GateSim: TannerLb\nettran\scmos\scms2sim.mac
- L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

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<tr>
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<th>Width</th>
<th>Area</th>
<th>Equivalent Gate</th>
<th>Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 µ</td>
<td>90 µ</td>
<td>27000 µ²</td>
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**Logic Equation**

N/A

**Delay Characteristics:**

N/A
This page is intentionally left blank.
**Description:** Pad Spacer with No Connection to Bonding Pad

**Library:** MOSIS TSMC 0.35P  
**Primitive Set:** Tanner SCMOS.Cells  
Tanner.TIB.Samples

**Schematic:** S-Edit  
**File:** TannerLb/scmos/mTSMs035P.sdb  
**Module:** N/A

**Mask layout:** L-Edit  
**File:** TannerLb/scmos/mTSMs035P.tdb  
**Cell:** PADNC

**Mapping Macros:**  
GateSim: TannerLb/nettran/scmos/scms2sim.mac  
L-Edit/SPR: TannerLb/nettran/scmos/scms2tpr.mac

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<th>Drive</th>
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**Logic Equation**

N/A

**Delay Characteristics:** N/A
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N/A
### Output Pad

**Description:** Output Pad with Buffer

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<td>Schematic File: TannerLb\scmos\mTSMs035P.sdb</td>
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#### Logic Symbol

```
DataOut
  |  |
  | Pad
PadOut_SCmos
```

#### Truth Table

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<th>D0</th>
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<td>1</td>
<td>1</td>
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#### Capacitance

N/A

#### Delay Characteristics:

\[
\begin{align*}
T_{pd} &= 1.92\text{ns} \\
T_r &= 1.48\text{ns} \\
T_f &= 1.23\text{ns}
\end{align*}
\]
PadOut

DataOut

Pad

PadBidirHE_SCMOS
**Power Pad**

**Description:** Power Pad

Library: MOSIS TSMC 0.35P  
Primitive Set: Tanner SCMOS.Cells  
Tanner.TIB.Samples

Schematic: S-Edit  
File: TannerLb\scmos\mTSMs035P.sdb  
Module: PADVDD

Mask layout: L-Edit  
File: TannerLb\scmos\mTSMs035P.tdb  
Cell: PADVDD

Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac  
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

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<th>Drive</th>
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**Logic Equation**

N/A

**Delay Characteristics:**

N/A
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