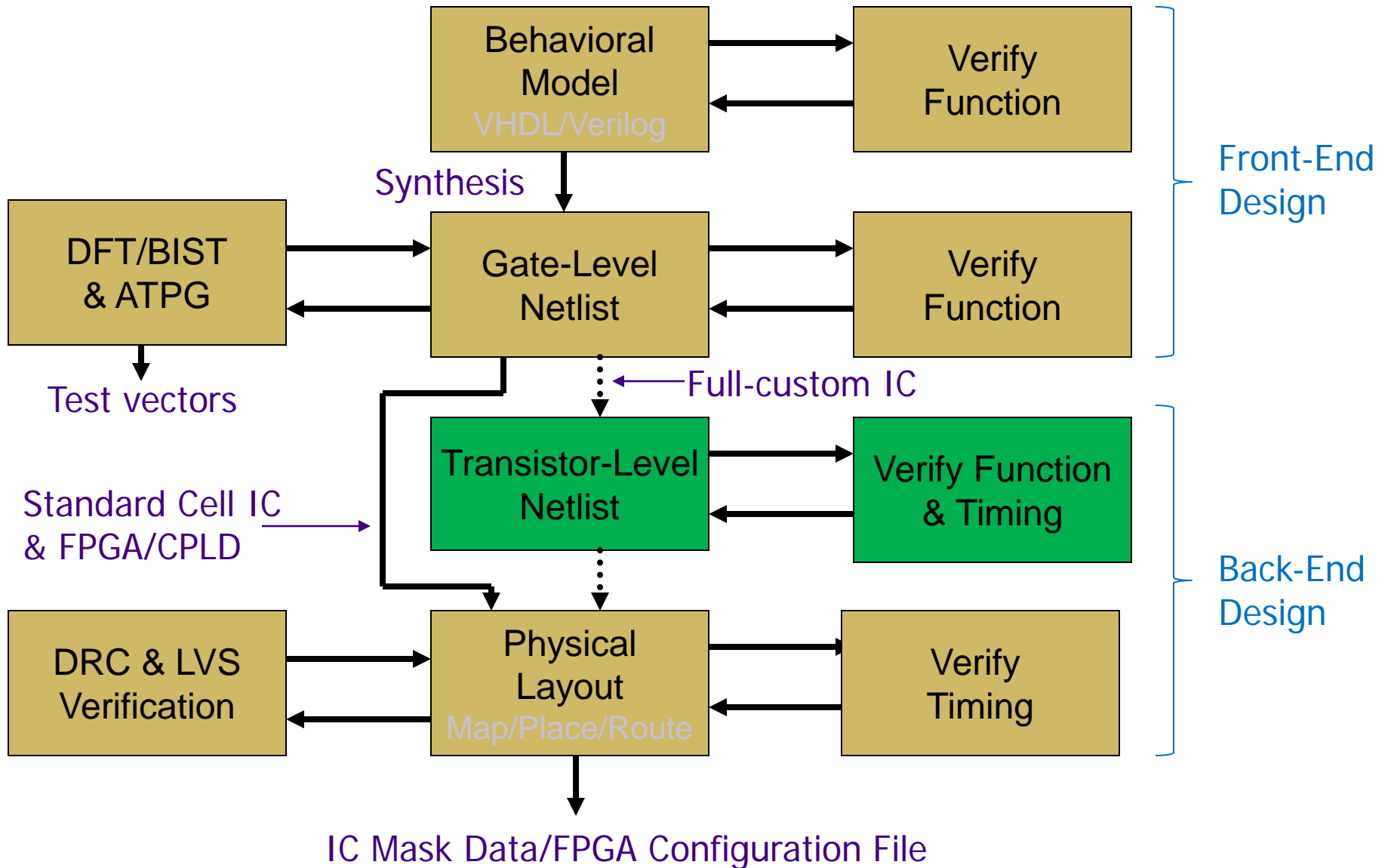


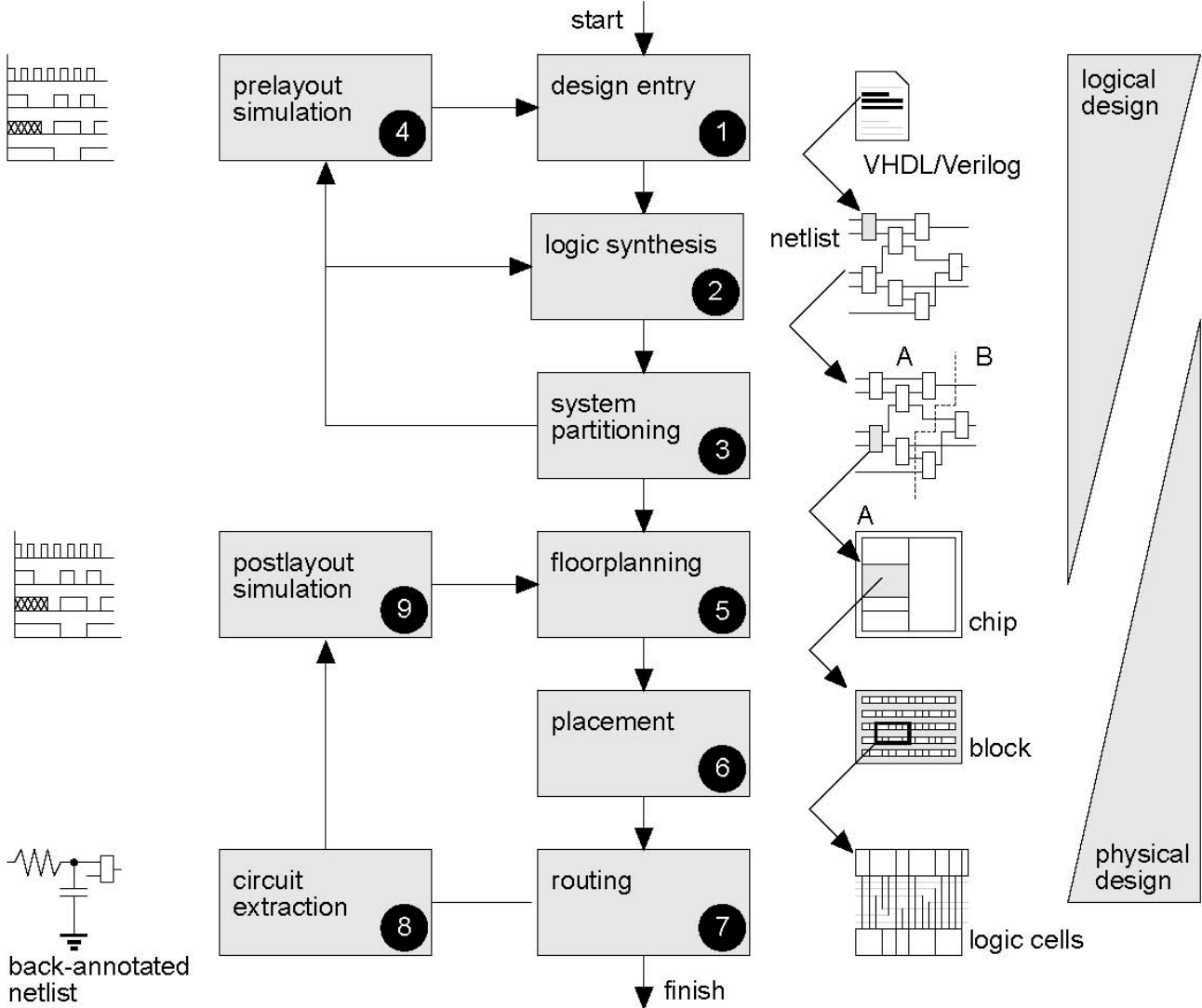
ASIC Computer-Aided Design Flow

ELEC 5250/6250 Lecture 3

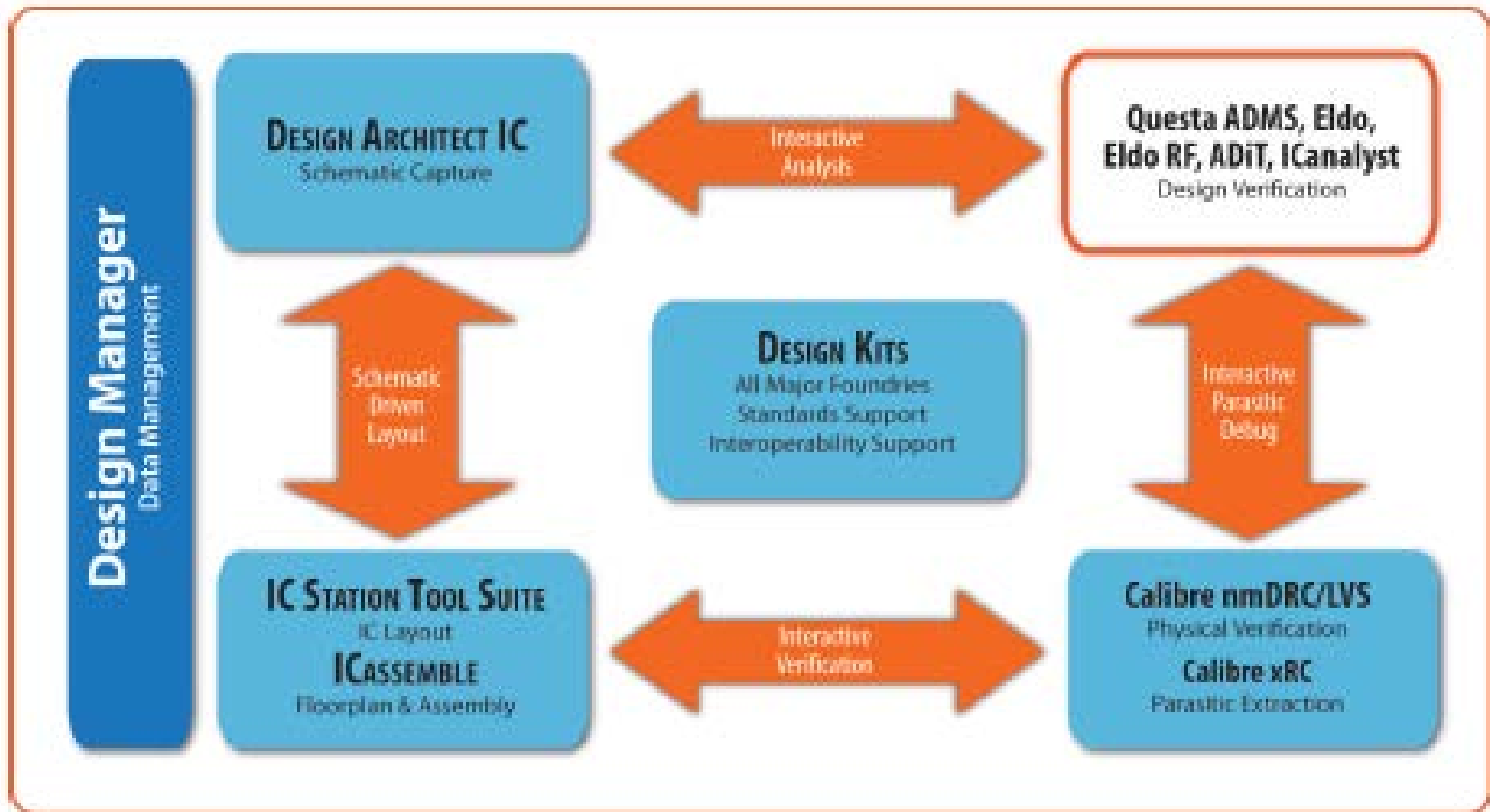
ASIC Design Flow



ASIC Design Flow



Mentor Graphics Analog/Mixed-Signal IC Design Flow



ASIC CAD tools available in ECE

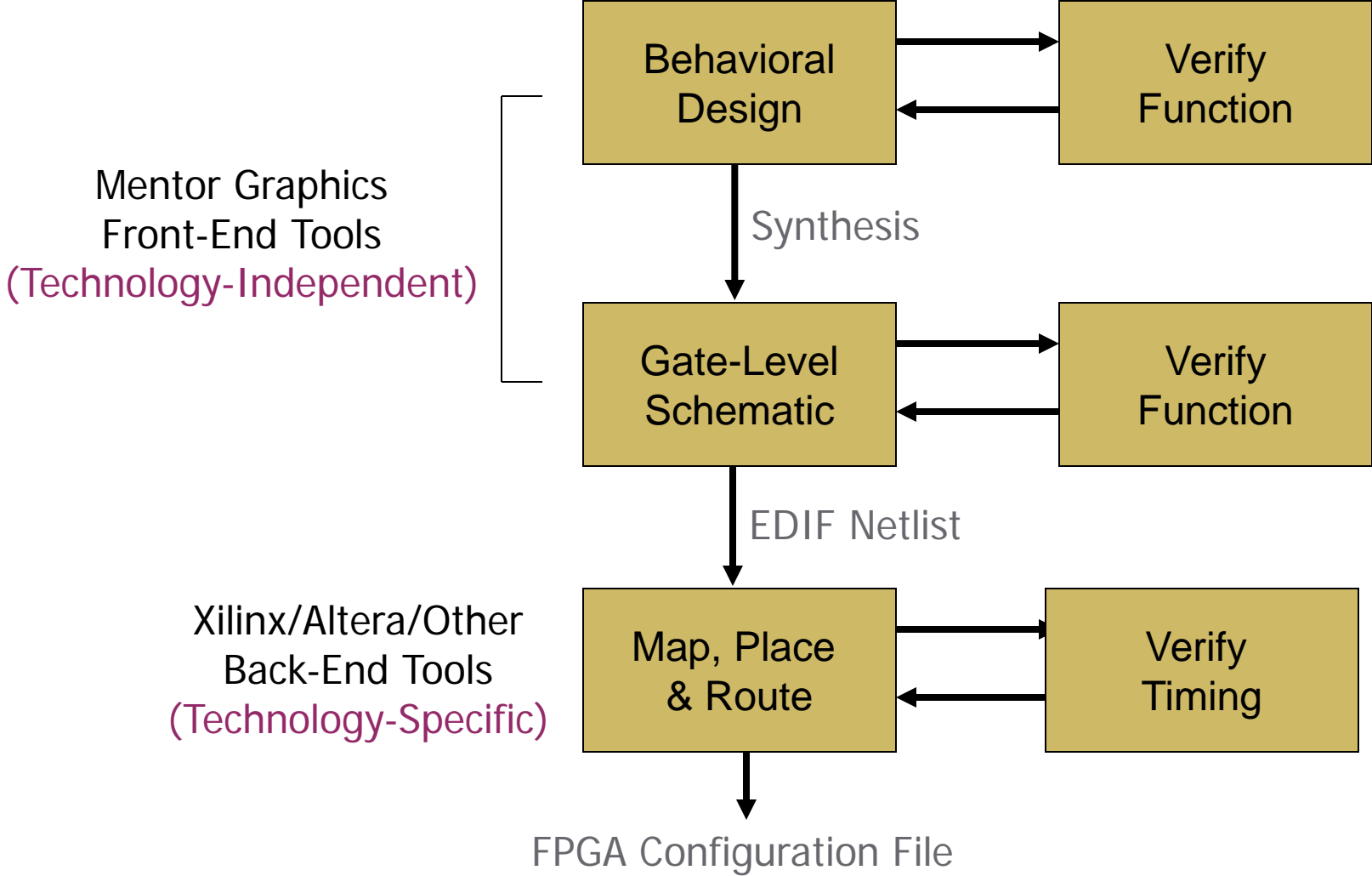
- Modeling and Simulation
 - Modelsim, Questa-ADMS, Eldo, ADiT (Mentor Graphics)
 - Verilog-XL, NC_Verilog, Spectre (Cadence)
- Design Synthesis (digital)
 - Leonardo Spectrum, Precision RTL (Mentor Graphics)
 - Design Compiler (Synopsys), RTL Compiler (Cadence)
- Design for Test and Automatic Test Pattern Generation
 - DFT Advisor, Fastscan (Mentor Graphics)
- Schematic Capture & Design Integration
 - Design Architect-IC (Mentor Graphics)
 - Design Framework II (DFII) - Composer (Cadence)
- Physical Layout
 - IC Station (Mentor Graphics)
 - SOC Encounter, Virtuoso (Cadence)
- Design Verification
 - Calibre (Mentor Graphics)
 - Diva, Assura (Cadence)

Mentor Graphics ASIC Design Kit (ADK)

- Technology files & standard cell libraries
 - AMI: ami12, ami05 (1.2, 0.5 μm)
 - TSMC: tsmc035, tsmc025, tsmc018 (0.35, 0.25, 0.18 μm)
- IC flow & DFT tool support files:
 - Simulation
 - VHDL/Verilog/Mixed-Signal models (*Modelsim SE/ADVance MS*)
 - Analog (SPICE) models (*Eldo/Accusim*)
 - Post-layout timing (*Mach TA*)
 - Digital schematic (*Quicksim II, Quicksim Pro*) (except tsmc025, tsmc018)
 - Synthesis to standard cells (*LeonardoSpectrum*)
 - Design for test & ATPG (*DFT Advisor, Flextest / Fastscan*)
 - Schematic capture (*Design Architect-IC*)
 - IC physical design (standard cell & custom)
 - Floorplan, place & route (*IC Station*)
 - Design rule check, layout vs schematic, parameter extraction (*Calibre*)

We also have ADK's for Cadence tools for several technologies

FPGA Design Flow



Xilinx/Altera FPGA/CPLD Design Tools

- Simulate designs in *Modelsim*
 - Behavioral models (VHDL, Verilog)
 - Synthesized netlists (VHDL, Verilog)
 - Requires “primitives” library for the target technology
- Synthesize netlist from behavioral model
 - *Leonardo (Levels 1,2,3)* has libraries for most FPGAs (*ASIC-only version currently installed*)
 - *Xilinx ISE* has its own synthesis tool
- Vendor tools for back-end design
 - Map, place, route, configure device, timing analysis, generate timing models
 - *Xilinx Integrated Software Environment (ISE)*
 - *Altera Quartus II & Max+Plus2*
- Higher level tools for system design & management
 - *Mentor Graphics FPGA Advantage*
 - *Xilinx Platform Studio* : SoC design, IP management, HW / SW codesign