

**ELEC 5250/6250 – COMPUTER-AIDED DESIGN OF DIGITAL LOGIC CIRCUITS**  
(Elective for ELEC, ECPE)

2011 Catalog Data: ELEC 5250/6250. COMPUTER-AIDED DESIGN OF DIGITAL LOGIC CIRCUITS (3) LEC. 3. Pr., ELEC 2220 or COMP 3350. Computer-automated design of digital logic circuits, using discrete gates, programmable logic devices, and standard cells, hardware description languages, circuit simulation for design verification and analysis, fault diagnosis and testing.

References: Mentor Graphics manuals and tutorials (College of Engineering Network)

Application-Specific Integrated Circuits, Michael J. S. Smith., Addison Wesley Longman, Inc., 1997. (2008 Soft cover edition available at Amazon.com, etc.)

**EDACafe:** <http://www.edacafe.com/>

**Chiptalk.org:** <http://www.chiptalk.org>

**Mentor Graphics:** <http://www.mentor.com>

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Course Web Page: [http://www.eng.auburn.edu/~nelson/courses/elec5250\\_6250](http://www.eng.auburn.edu/~nelson/courses/elec5250_6250)

References: Links to CAD tool tutorials provided on course web page.

Course Objectives:

1. To be able to use computer-aided design tools for development of complex digital logic circuits
2. To be able to model, simulate, verify, analyze, and synthesize with hardware description languages
3. To be able to design and prototype with standard cell technology and programmable logic
4. To be able to design tests for digital logic circuits, and design for testability

Prerequisites by topic:

1. Digital logic design and analysis or switching theory
2. Computer system organization and design

Topics:

1. ASIC design options and physical implementation options
2. Hierarchical design concepts and CAD flow for digital ASICS
3. Hardware description languages
4. VHDL entities, architectures, and processes
5. VHDL modeling for combinational and sequential circuits
6. Logic synthesis from VHDL models
7. Gate-level modeling, design capture
8. Design simulation for verification and analysis
9. Programmable logic: PLAs, PLDs, CPLDs and FPGAs
10. Placement and routing of FPGAs
11. Design with standard cells
12. Placement and routing of standard-cell designs
13. Chip floor planning, placement and routing
14. Digital testing
15. Fault modeling and fault simulation
16. Design for testability
17. CAD tools for testing

Method for evaluating student performance:

Midterm exam	20%
Final exam	20%
Design projects	60%

Design Projects:

Following a series of “introductory” projects, a specification-oriented design project will be an integral part of the course which will include design, modeling, simulation, and synthesis of VHDL into standard cells and, time permitting, a field programmable gate array. Students in ELEC 5250 and 6250 will be assigned different projects. The design project will include development of test vectors and fault simulation analysis of the test vectors and design.

**Every student is expected to do his/her own project. Discussion of various aspects of the project with fellow students is acceptable, provided that designs are neither collaborative nor copied.**

Class attendance: Class attendance is encouraged, but will not be accounted for in the course grade.

Policy on unannounced quizzes: There will be no unannounced quizzes.

Special Accommodations: Any student requiring special accommodations should come by the instructor’s office within the first two days of class, bringing your letter from the Office of Students with Disabilities.

Contribution of course to meeting the professional component

Engineering topics: 3 credits  
33% engineering science (1 credit)  
67% engineering design (2 credits)

Primary program outcomes related to this course:

- Outcome 1. Ability to apply knowledge of math, science and engineering to solve problems.
- Outcome 2. Ability to apply in-depth knowledge in one or more disciplines
- Outcome 3. Ability to design an electrical component or system to meet desired needs.
- Outcome 6. Proficiency in the use of computers and other modern tools to solve engineering problems.

Prepared by: V. P. Nelson

Date: August 18, 2011