

ELEC 6250 – Final Project/Exam – Fall Semester 2011
Due Friday, December 2, 4:00 p.m.

You are to modify your previously-designed divider circuit to incorporate “full-scan” design, and then redo the block layout and analyses. Note that this is for the circuit block only, and not the top-level chip. As a minimum, you must provide the following information:

1. Comparison of the area of the physical circuit block layout for the original design (non-scan) vs the full-scan design (determine the area penalty incurred by using scan design).
2. Comparison of the worst case clock to output pin delay and maximum clock frequency for the non-scan vs. the full-scan design (determine the performance penalty incurred by using scan design.)
3. Simulation results showing the application of test patterns produced by ATPG tool and the resulting circuit outputs.

Create a report (to be submitted electronically) describing each of the design steps used to produce the above information. For each design step, briefly describe what was done, and how you verified the results of that design step. You must provide sufficient evidence in your report to convince me of the correctness of each step in your design process. A list of required evidence is purposely not provided here. You are expected to be able to determine what information should be generated and examined to verify each design step.

If you feel that your divider circuit cannot be completed to do the required analyses, you may do the above with the modulo-6 counter instead, with a one-letter-grade penalty on the final exam score.