

ELEC 5250 – Final Exam/Project – Fall Semester 2011
Due Friday, December 2, 4:00 p.m.

You are to modify your modulo-7 counter circuit to incorporate full-scan design, and then redo the block layout and analysis as follows. The report is to be submitted electronically.

1. Use “DFTadvisor” to convert your circuit from non-scan to full-scan design. Submit the new Verilog netlist model, and the corresponding schematic diagram from Design Architect-IC.
2. Use “FastScan” to generate a complete test set for the modified counter circuit. Submit the “statistics” from the ATPG and fault simulation, showing the number of faults detected vs. total number of assumed faults.
3. Perform a behavioral simulation of the modified counter circuit, using the test patterns generated by “FastScan” (save the patterns in VHDL or Verilog form). Submit the simulation results, showing the primary inputs and outputs. This is what the manufacturing test should look like.
4. Generate a new layout for the modified counter circuit, and perform design rule and LVS checks. Measure and compare the areas of the non-scan and full-scan layouts, and determine the percent increase in area, i.e. the “area overhead” due to the use of full-scan design.
5. Determine and compare the worst case clock to output delay and clock to flop-flop inputs path (which determines max clock frequency) for the non-scan and full scan designs, using ADiT to simulate and measure these parameters on the post-layout circuit models. These indicate the “performance penalties” due to the use of full-scan design.