

"Super-SPARC"
 p1P
 (Texas + SUN)

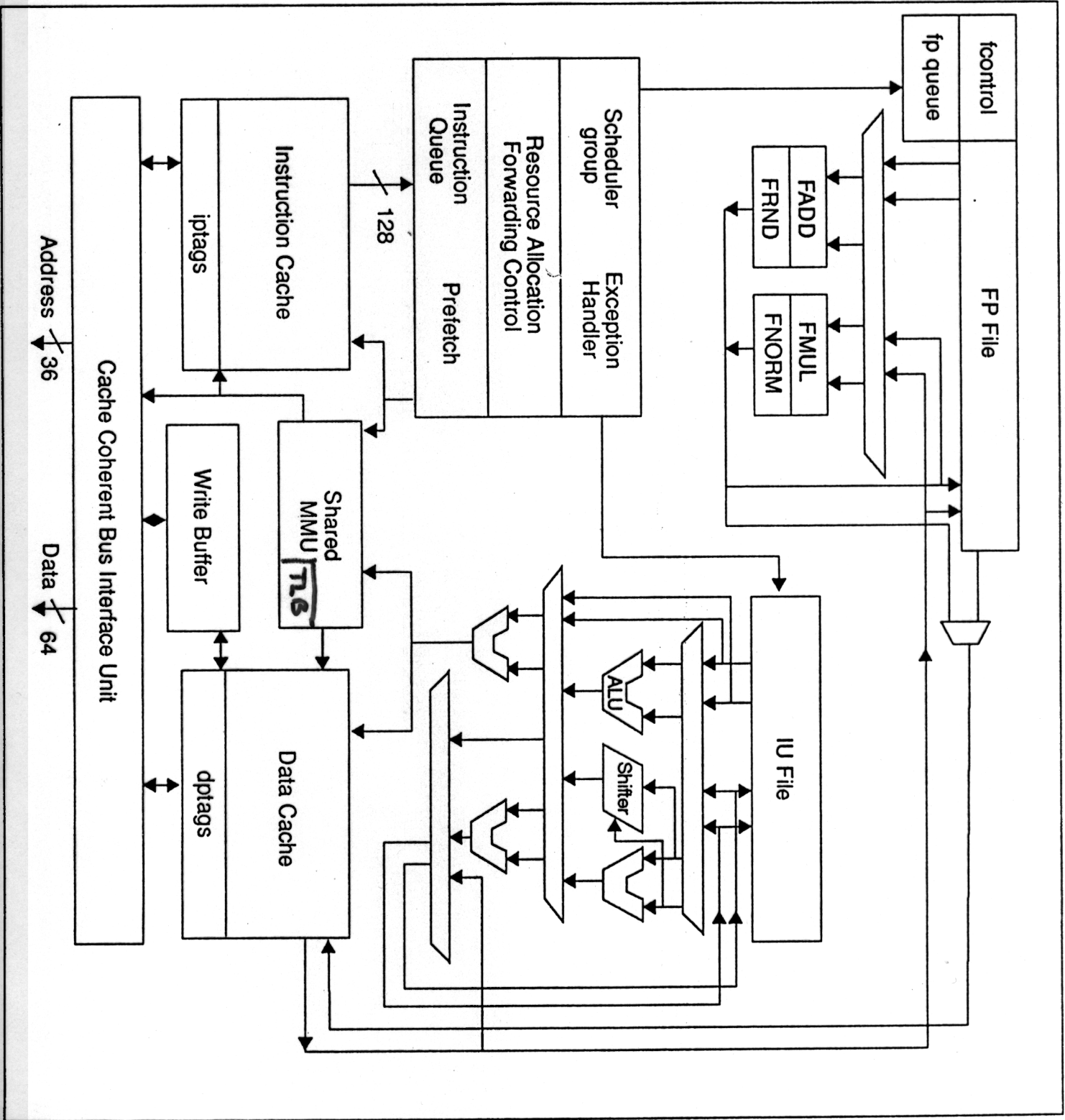


Figure 2-1 Functional Block Diagram

Pipeline Organization

The SuperSPARC processor [ISSCC 1992], [Compton 1992] uses a four-cycle integer pipeline. Each cycle has two-phases. The first cycle (F0, F1) fetches up to four instructions from the first-level instruction cache into an instruction queue. There are three phases of decode (D0, D1, D2), two stages of execution (E0, E1) and a writeback stage (WB).

Table 3-1 Pipeline stages

Stage	Activity
F0	I-cache ram access I-cache TLB lookup
F1	I-cache match detect 4 instructions sent to the iqueue
D0	Issue 1,2 or 3 instructions Select register file indices for LD/ST address registers
D1	Read Rfile for LD/ST address registers Resource allocation for ALU instructions Evaluate branch target address
D2	Read Rfile for ALU operands Add LD/ST address registers to form effective address
E0	1st stage of ALU D cache RAM access D cache TLB lookup FP instruction dispatch
E1	2nd stage of ALU D cache match detect Load data available Resolve exceptions
WB	Write back into the Rfile Retire store into the store buffer

The operation of the pipeline is illustrated by the execution of a load instruction with a forwarding path in Figure 3-1. The pipeline stages are detailed in Table 3-1.

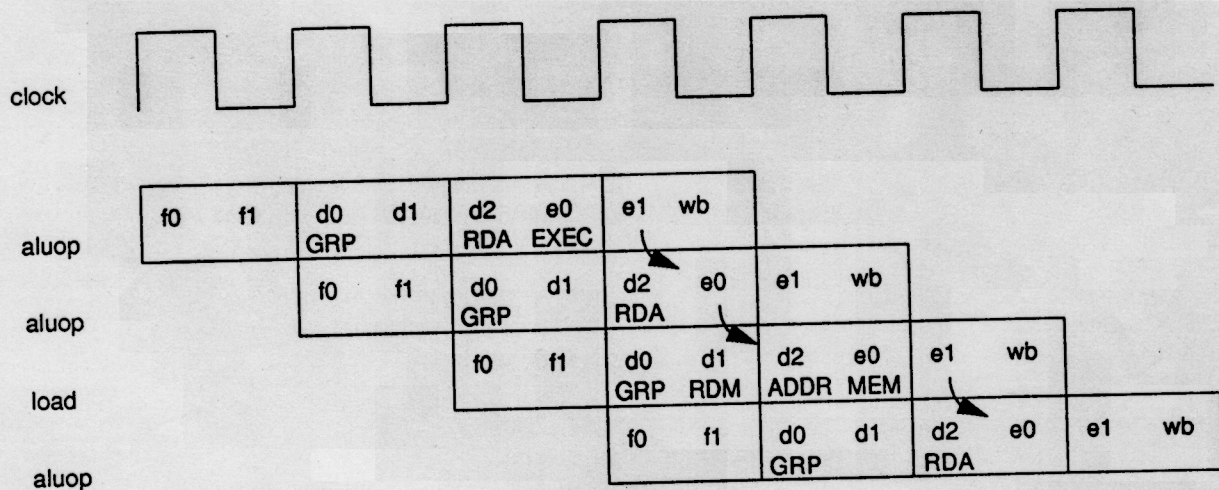


Figure 3-1 Pipelined Execution of Load with Forwarding