

Figure 1. MPC601 Block Diagram

MPC 601 CACHE

32 kbyte unified 8-way set-associative

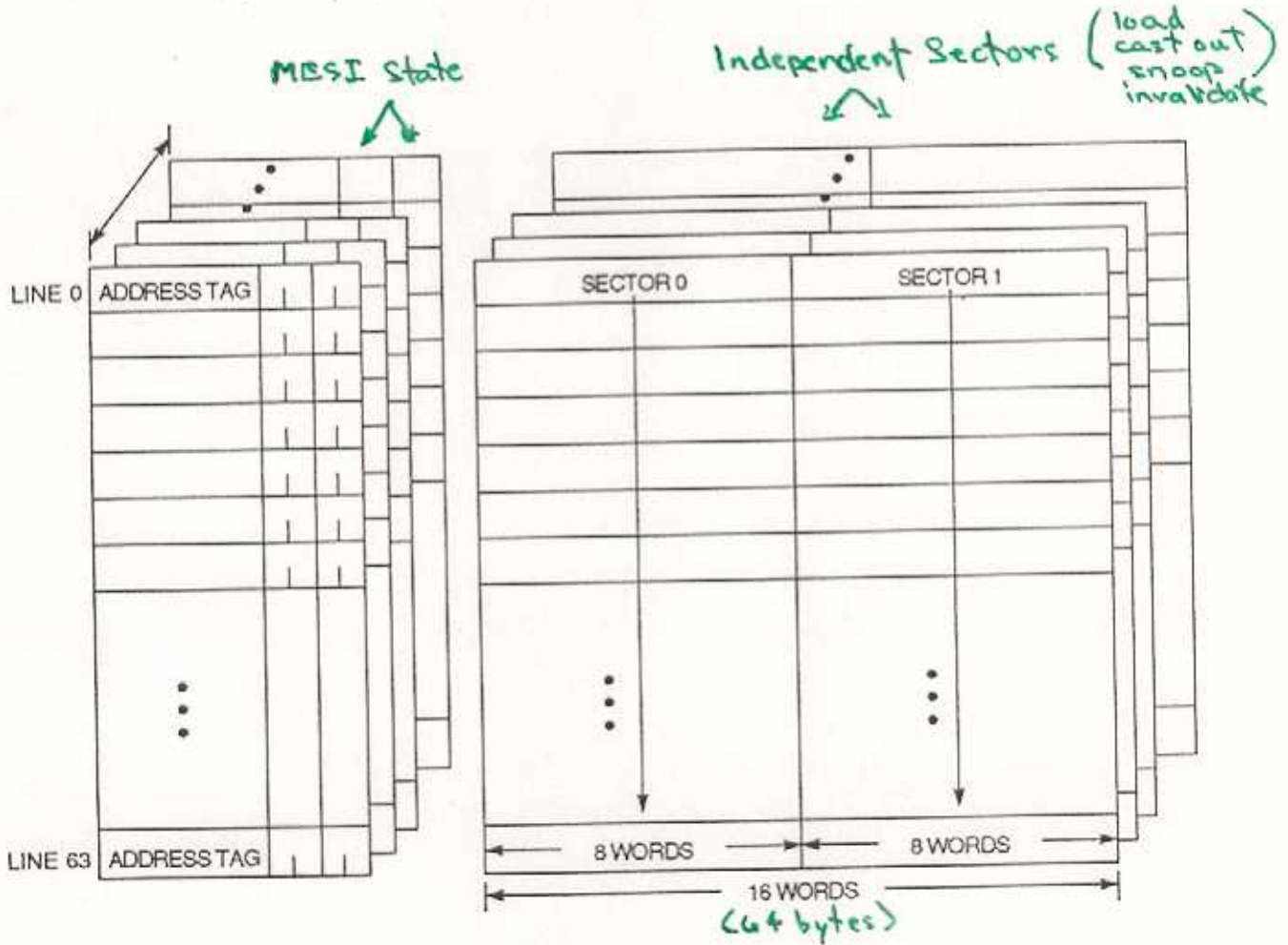
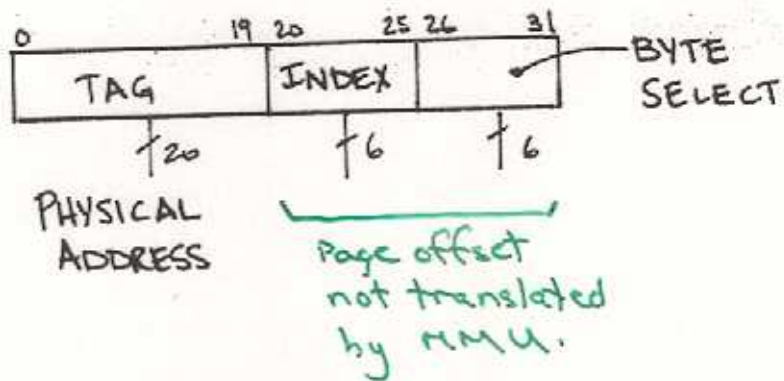


Figure 1-4. Cache Unit Organization



MPC601 A 32-Bit PowerPC Implementation

Cache

32 kbyte 8-way set-associative unified cache
write-back / write-through modes programmable on per-page or per-block basis
MESI protocol used for coherency in multiprocessor environment
cacheable unit = 1 sector = (8) 32-bit words
LRU replacement
snooping logic has separate port into cache so snooping doesn't affect system performance
complete read-modify-write operation to cache can be performed each cycle
external cache loads always transfer critical quad-word first (can be forwarded) then other

Cache arbitration

cache can be accessed by:

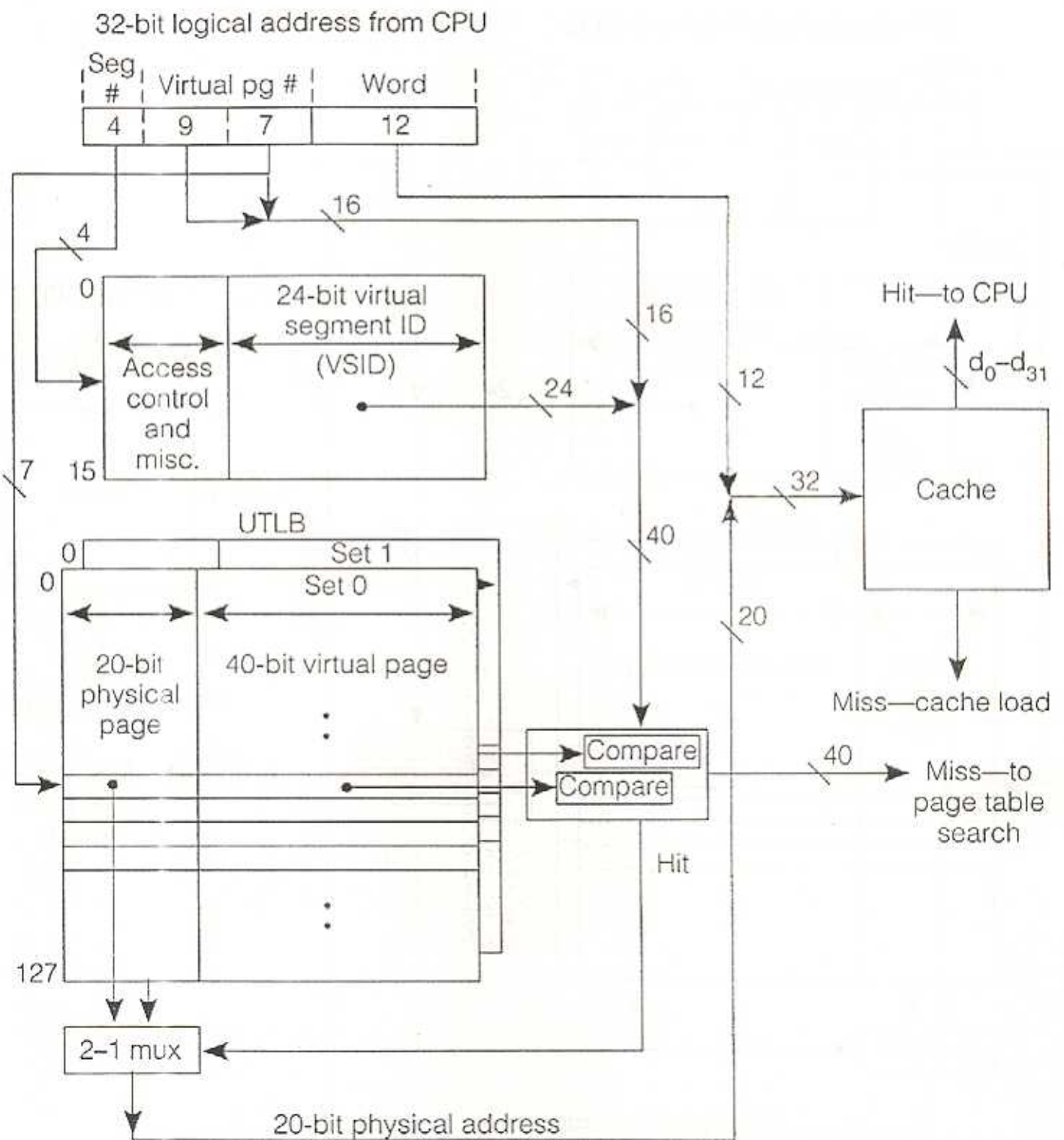
- integer unit
- instruction unit
- preceding cache operation (re-load)
- bus snooping logic

Cache access priorities:

1. Cache Reloads
2. Second-cycle cast-out operations when the additional sector is modified
3. Snoop requests - generate a cache sector push operation
4. Floating point store
5. Integer operand retries
6. Integer unit requests
7. Instruction fetches

MPC603 - Two caches, 8K, 32 bytes/line, 2-way set assoc.
MPC604 - " 16K, 32 " , 4-way " "
MPC620 - " 32K, 64 " , 8-way " "

Power PC 601 MMU Operation



- 32 bit logical address (from 52-bit Virtual Addr.)
- 4KB page size (2^{12})
- 256MB segment size (2^{28})
- 128KB \rightarrow 8MB blocks

3 TLB's:

① ITLB (Instruction only)

4 entry full-associative
holds addr. translation for last 4 instr.
LRU

② UTLB

256 entry
2-way set-associative

Block

③ BTLB

4 BAT reg.
Maintain with software
Available block translations.

(use either blocks or pages)

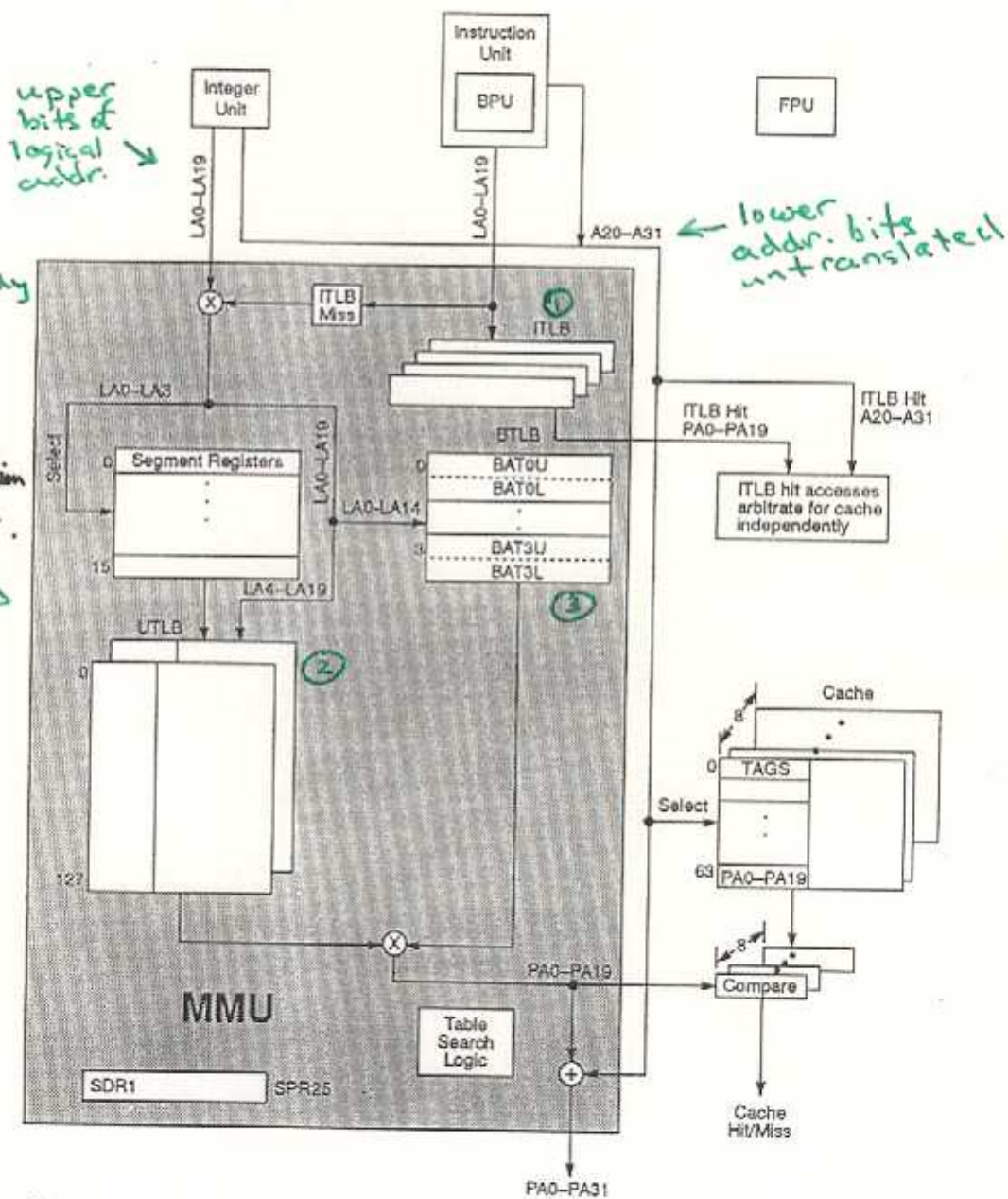


Figure 6-1. MMU Block Diagram