

ELEC 5200/6200 – COMPUTER ARCHITECTURE AND DESIGN
Spring Semester, 2006

2005 Catalog Data: ELEC 5200/6200. COMPUTER ARCHITECTURE AND DESIGN (3) LEC. 3. Pr., ELEC 2220. Structural organization and hardware design of digital computers; register transfers; micro-operations, control units and timing; instruction set design; input/output devices, multiprocessors, automated hardware design aids.

Textbook: Computer Organization & Design: The Hardware/Software Interface, 3rd Ed., D.A. Patterson & J.L. Hennessy, Morgan Kaufmann Publishers, 2005.

References: Documents posted at http://www.eng.auburn.edu/~nelson/courses/elec5200_6200

VHDL Tutorial & VHDL Design & Simulation with ModelSim EE Tutorial on line at: <http://www.eng.auburn.edu/ece> (Click on Computing Tools & select from list)

VHDL Interactive Tutorial (from IEEE). on line at: <http://www.eng.auburn.edu/ece> (Click on Computing Tools & select from list)

Coordinator: Victor P. Nelson, Professor of Electrical & Computer Engineering

Goals: To introduce the student to design principles applied to the design of computer systems and the implementation of digital computer hardware.

Prerequisites by topic:

1. Combinational and sequential logic circuit design
2. Computer organization
3. Assembly and machine language programming

Topics:

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| 1. | History of computer architecture (2 classes) | 1.1 - 1.7 |
| 2. | Hardware modeling with VHDL (6 classes) | VHDL Tutorials |
| 3. | Instruction set characteristics and design (5 classes) | 2.1 – 2.9, 2.16 |
| 4. | Arithmetic and logic unit design (4 classes) | 3.1 – 3.5 |
| 5. | Floating-point hardware (1 class) | 3.6 - 3.7 |
| 6. | Computer system performance (2 classes) | 4.1 - 4.6 |
| 7. | Single-cycle CPU design (3 classes) | 5.1 - 5.4 |
| 8. | Multi-cycle CPU design (2 classes) | 5.5 - 5.7 |
| 9. | Pipelined datapath and control (3 classes) | 6.1 - 6.7 |
| 10. | Memory hierarchies (2 classes) | 7.1, 7.5 |
| 11. | Cache memory systems (3 classes) | 7.2 - 7.3 |
| 12. | Virtual memory system design (3 classes) | 7.4 |
| 13. | Input/output buses and device interfacing (2 classes) | 8.1 - 8.7 |
| 14. | Multiprocessor system architectures (1 classes) | 9 (on CD) |
| 15. | Exams and review (3 classes) | |

Method for evaluating student performance:

Hour quizzes (2 @ 100 points)	200 points
Final exam	150 points
Paper	20 points
CPU design projects	<u>100 points</u>
TOTAL	470 points

Homework:

Problems from the textbook will be assigned throughout the quarter to reinforce the class material. However, submission of these for critique and correction is optional.

Computer Design Project:

A small RISC CPU will be designed in the VHDL modeling language and verified via Mentor Graphics "ModelSim EE" simulator on SUN workstations. The project will be due on the last class day. Parts of it will be assigned, collected, and graded throughout the quarter. 80% of the project grade will be from these individual parts; the other 20% of the project grade will be for the final project and simulation. Project grades will include components for correctness of design, modeling technique, testing, and documentation.

Projects will be different for ELEC 5200 and ELEC 6200.

Note that every student is expected to do his/her own project. Discussion of various aspects of the project with fellow students is acceptable, provided that designs are not copied. Copying of another student's project will be considered a violation of the academic honesty code by both students, and will be dealt with as outlined in the "Tiger Cub".

Class attendance: Class attendance is encouraged but will not be accounted for in the course grade.

Policy on unannounced quizzes: There will be no unannounced quizzes.

Special Accommodations: Any student requiring special accommodations should come by my office within the first two days of class, bringing your letter from the Office of Students with Disabilities.