

**ELEC 6200 - FINAL PART OF PROJECT**  
**Final Project Due: Monday, May 1**

1. A sample VHDL **Memory** model (mips\_memory\_bin.vhd) is available on the class web page for you to adapt for your project. This model contains code to load a test program, at the start of simulation, from an object-code file named “testprog”. This object-code file is simply a list of binary numbers, one per line, to be loaded into contiguous memory locations, beginning at address 0. See the example “testprog” file provided for the MIPS test program for the ELEC 5200 students.
2. Create a “**System component**” by adding control logic to your pipelined CPU, along with instruction and data memory components, if you did not already do so in the previous project. A clock input should be the only external port of this "System". If you wish, you may build a “clock generator” into the system and omit the clock port.

Example: `clk <= not clk after 50ns; -- Clock with period 100ns`

3. A test program will be supplied. You will need to create the object-code file “program” for this test program (hand-compile the program into binary object code). Each line must begin with the 14-bit binary code for one instruction or data value to be loaded into memory. The rest of the line after the binary code is ignored by the model, so you can put text there as “comments”. I suggest putting the “assembly language” equivalent of that binary instruction.  
Example: `10011100001111          add r1,r2,r3`
4. For the **final simulation**, to minimize the size of the listing, display only **one line per clock transition** (i.e. trigger only on clock signal transitions). Show a sufficient set of signals to demonstrate correct operation of each instruction (control unit state, address bus, data bus, ALU output, register file outputs, register file input, memory control signals, etc.) Don’t show the entire register file. On the simulation listing, annotate by writing the corresponding assembly language instruction next to each execute cycle and highlighting the “significant” result register or bus value.