

ELEC 6200 PROJECT #5

Due: Wednesday, April 12

Design and test a VHDL model of your pipelined CPU datapath, as described by the block diagram and register transfers of Project 4. The datapath should have the various control and status signals as external “ports” in the decode stage. These will be connected to a Control Unit in the final project. Test the datapath by forcing control inputs to selected values (mimic the operation of a control unit).

Notes:

1. This is to be a register-transfer-level design - not gate level.
2. The top-level design should contain **only component instantiations**, matching your block diagram (changes may be made to the block diagram as necessary).
3. Design and test VHDL models of each unique component used in your datapath. **Use previously-designed components** from your library whenever possible (adders, multiplexers, etc.).
4. Create a **table** listing all control signals and the values of each control signal required for each stage of the pipeline for each of the instruction types. (List the fetch and decode stage only once.)

Major Datapath Components Likely to be Needed:

- ❖ **ALU/Adder(s)**. These can be derived from the adder/subtractor of Project 1. The main ALU should not provide unnecessary functions.
- ❖ **Pipeline registers**: These should be simple edge-triggered registers.
- ❖ **Register file**: Design as a multi-port “memory array”. **DO NOT** instantiate individual registers!
- ❖ **Program and data memories**: Base these on the memory models discussed in class.
- ❖ **Sign/zero extension logic**, as appropriate, for ALU inputs.
- ❖ **Program counter (PC)** – this should be a “simple register”.
- ❖ Assorted **multiplexers** for data paths and register address inputs.

Thoroughly simulate each new component individually, before inserting it into the datapath. Annotate and submit each simulation.

Simulate the datapath component to verify all required register transfers by applying control signals with force commands, as they would normally be applied by the control unit. **Use your control signal table from Note (4) above to design the datapath test, and show in the simulation where you verified each required register transfer for the CPU.** (If some register transfers are common to multiple instructions, you do not need to show them separately for every instruction – but it might be a good idea to do so anyway.)