

ELEC 6200 Project #4
Due: Friday, March 17, 2006

Design the datapath of a pipelined CPU that will realize the instruction set architecture (ISA) designed in the previous assignment (including any “adjustments” made to the ISA). You may choose the number of states in the pipeline.

For your instruction set architecture, provide the following:

1. A block diagram (register level) of the datapath, with all components and control signals clearly labeled. Also show and label the stages of your pipeline.
2. A description of the function of each component in the datapath.
3. For each instruction of your ISA, list the register transfers, or sequence of register transfers, required to fetch and execute the instruction. Register names should correspond to components in your datapath diagram.
4. A discussion of the tradeoffs and other design decisions made in developing your datapath. This should include:
 - Cost vs. speed tradeoffs that you considered.
 - How you selected the number of pipeline stages.
 - Selection of edge-triggered vs. latching registers.
 - Other decisions that were considered.

The next assignment will be to design a VHDL model of your datapath. You might want to start on that as soon as you have this assignment completed.