

ELEC 5200 Project #4
Due: Friday, March 17, 2006

Design a datapath of a CPU that will realize a subset of the MIPS R2000 instruction set architecture (ISA). The ISA is to be limited to the following instructions:

- Load/Store: LW,SW,LUI
- Arithmetic: ADD, ADDI, SUB
- Logical: AND,ANDI,OR,ORI
- Set Conditionally: SLT,SLTI
- Conditional Branch: BEQ,BNE
- Jump/Call: J,JR,JAL

For this instruction set architecture, provide the following:

1. A block diagram (register level) of the datapath, with all components and control signals clearly labeled. Use a multi-cycle design in which each instruction takes exactly two clock cycles to fetch and execute: one to fetch the instruction and one to execute the instruction.
2. A description of the function of each component in the datapath.
3. For each instruction of your ISA, list the register transfers, or sequence of register transfers, required to fetch and execute the instruction. Register names should correspond to components in your datapath diagram.
4. A discussion of the tradeoffs and other design decisions made in developing your datapath. This should include:
 - Cost vs. speed tradeoffs that you considered.
 - Why you chose a single-cycle or multi-cycle design (option #1 only)
 - Decisions related to “shared” and/or “dedicated” components.
 - Selection of edge-triggered vs. latching registers.
 - Other decisions that were considered.

The next assignment will be to design a VHDL model of your datapath. You might want to start on that as soon as you have this assignment completed.