## Progress of State of the Art

<table>
<thead>
<tr>
<th>Year</th>
<th>Integration Level</th>
<th># devices</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1938-46</td>
<td>Electromagnetic relays</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1943-54</td>
<td>Vacuum tubes</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1947-50</td>
<td>Transistor invented</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1950-61</td>
<td>Discrete components</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1961-66</td>
<td>SSI</td>
<td>10’s</td>
<td>Flip-flop</td>
</tr>
<tr>
<td>1966-71</td>
<td>MSI</td>
<td>100’s</td>
<td>Counter</td>
</tr>
<tr>
<td>1971-80</td>
<td>LSI</td>
<td>1,000’s</td>
<td>uP</td>
</tr>
<tr>
<td>1980-85</td>
<td>VLSI</td>
<td>100,000’s</td>
<td>uC</td>
</tr>
<tr>
<td>1985-90</td>
<td>ULSI*</td>
<td>1M</td>
<td>uC*</td>
</tr>
<tr>
<td>1990</td>
<td>GSI**</td>
<td>10M</td>
<td>SoC</td>
</tr>
<tr>
<td>2011</td>
<td>Intel Ten-Core Xeon</td>
<td>2.6G</td>
<td>CPU</td>
</tr>
<tr>
<td>2017</td>
<td>Nvidia GV100 Volta</td>
<td><strong>21.1G</strong></td>
<td>GPU</td>
</tr>
</tbody>
</table>
Intel® Core™ i7 Processor

Performance/Features:
- 8 processing threads via Intel® Hyper-Threading Technology (HT)
- 4 cores
- Turbo Mode operation
- Intel® QuickPath Interconnect (Intel® QPI) to Intel® X58 Express Chipset
- Integrated Memory Controller (IMC) – 3ch DDR3
- 7 more SSE4 instructions
- Overspeed Protection Removed

Intel’s Next Gen Computing Genius!
Apple “A8” SoC (System on Chip)

- Used in iPhone6 & iPhone6 Plus
- Manufactured by TSMC
  - 20nm, 89mm², 2B transistors
- Elements (unofficial):
  - 2 x ARM Cyclone ARMv8 64-bit cores running at 1.4GHz
  - IMG PowerVR 4-core GX6450 GPU
  - L1/L2/L3 SRAM caches
- Other devices
  - 1 GB LPDDR3 SDRAM
  - 16 to 128GB flash
  - Qualcomm MDM9625M LTE modem
  - M8 motion coprocessor (ARM Cortex M3 uC)
  - iSight camera
  - Near field communications chip (for Apple Pay)
  - User interface and sensors, accelerometers, gyro
  - Wi-Fi and Bluetooth
## SoC Example: NVIDIA Tegra 2

<table>
<thead>
<tr>
<th>Designer</th>
<th>NVIDIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year</td>
<td>2010</td>
</tr>
<tr>
<td>Processor</td>
<td>ARM Cortex-A9</td>
</tr>
<tr>
<td></td>
<td>(dual-core)</td>
</tr>
<tr>
<td>Frequency</td>
<td>Up to 1.2 GHz</td>
</tr>
<tr>
<td>Memory</td>
<td>1 GB 667 MHz LP-DDR2</td>
</tr>
<tr>
<td>Graphics</td>
<td>ULP GeForce</td>
</tr>
<tr>
<td>Process</td>
<td>40 nm</td>
</tr>
<tr>
<td>Package</td>
<td>12 x12 mm (Package on Package)</td>
</tr>
<tr>
<td>Used in tablets</td>
<td>Acer Iconia Tab A500</td>
</tr>
<tr>
<td></td>
<td>Asus Eee Pad Transformer</td>
</tr>
<tr>
<td></td>
<td>Motorola Xoom</td>
</tr>
<tr>
<td></td>
<td>Motorola Xoom Family Edition</td>
</tr>
<tr>
<td></td>
<td>Samsung Galaxy Tab 10.1</td>
</tr>
<tr>
<td></td>
<td>Toshiba Thrive</td>
</tr>
</tbody>
</table>

TI smartphone reference design

Main SoC
Internet of Things (IoT)

Socio-Economic Benefits

- **Automation** (higher productivity)
- **Smart monitoring, control and maintenance** (higher efficiency, lower cost, higher quality, better optimisation/outcomes)
- **Better safety** (early warning)
- **Higher responsiveness** (dynamic response to varying demands)
- **Huge and varied applications in industry, agriculture, health, transport, infrastructure, smart living, consumer etc.**
Digital integrated circuit design process

- **Requirements & Specifications**
- **Architectural Design**
- **Functional Design**
- **Logic Design**
- **Physical Design**
- **Fabrication Process**
- **Wafer Level Testing**
- **Saw Apart Packaging & Testing**

- **System Level**
- **Register Level**
- **Gate Level**
- **Transistor Level**

- **Behavioral Simulation (VHDL)**
- **Functional Simulation (RTL - VHDL/Verilog)**
- **Logic Simulation (VHDL/Verilog)**
- **Circuit Simulation (PSPICE)**

- **Fault Simulation (gate level fault model)**
- **Fault Simulation (transistor level fault model)**

- **Note all the simulation** (design verification) - helps to ensure the design works and assists in debugging design errors
- **To simulate a circuit, we must describe it in a manner that can be interpreted and understood by the simulator (HDL/netlist)**
Digital ASIC Design Flow

- **ELEC 4200 Activity**
- **Behavioral Model**: VHDL/Verilog
- **Gate-Level Netlist**
- **Transistor-Level Netlist**
- **Physical Layout**: Map/Place/Route
- **Full-custom IC**
- **DFT/BIST & ATPG**
- **Verify Function**
- **Verify Function & Timing**
- **Verify Timing**
- **DRC & LVS Verification**
- **IC Mask Data/FPGA Configuration File**

**Front-End Design**
- **Synthesis**
- **Test vectors**
- **Standard Cell IC & FPGA/CPLD**

**Back-End Design**
- **Physical Layout**
- **Verify Function**
- **Verify Function & Timing**
- **Verify Timing**
FPGA/CPLD Design Flow

Aldec/Mentor Graphics Front-End Tools (Technology-Independent)

Xilinx/Altera Back-End Tools (Technology-Specific)

Behavioral Design → Verify Function

Synthesis

Gate-Level Schematic → Verify Function

EDIF Netlist

Map, Place & Route → Verify Timing

FPGA Configuration File
Xilinx/Altera FPGA/CPLD Design Tools

- Create HDL model of design behavior/structure
  - Xilinx “Vivado” - *Integrated Software Environment*
  - Context-sensitive text editor
- Simulate designs in *Active-HDL* or *Modelsim*
  - Behavioral models (VHDL, Verilog)
  - Synthesized netlists (VHDL, Verilog)
    - Requires “primitives” library for the target technology
- Synthesize primitive-level netlist from a behavioral model
  - Xilinx *Vivado* has its own synthesis tool
  - Leonardo (Levels 1, 2, 3) has libraries for most FPGAs *(ASIC-only version currently installed)*
- Vendor tools for back-end design
  - Map, place, route, configure device, timing analysis, generate timing models
  - Xilinx *Vivado* - formerly *Integrated Software Environment* (ISE)
  - Altera *Quartus II & Max+Plus2*
- Higher level tools for system design & management
  - Xilinx *Platform Studio*: SoC design, IP management, HW/SW codesign
  - Mentor Graphics *FPGA Advantage*
Field Programmable Gate Arrays

- Configuration Memory
- Programmable Logic Blocks (PLBs)
- Programmable Input/Output Cells
- Programmable Interconnect

Typical Complexity = 5M – 1B transistors
Xilinx Zynq SoC devices

Zynq-7000 SoC: Dual-core ARM Cortex-A9 MPCore (up to 1GHz)
Zynq UltraScale+ MPSoC:
- Quad-core ARM Cortex-A53 MP (up to 1.5 GHz)
- Dual-core ARM Cortex-R5 MPCore (up to 600MHz)
- GPY ARM Mali-400 MP2 (up to 667MHz)
Zynq-7000 SoC Processor System
**Xilinx FPGA families (2015)**

<table>
<thead>
<tr>
<th></th>
<th>Spartan-6</th>
<th>Artix-7</th>
<th>Kintex-7</th>
<th>Virtex-7</th>
<th>Kintex Ultra Scale</th>
<th>Virtex Ultra Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>147,443</td>
<td>215,360</td>
<td>477,760</td>
<td>1,954,560</td>
<td>1,160,880</td>
<td>4,432,660</td>
</tr>
<tr>
<td>Block RAM</td>
<td>4.8 Mb</td>
<td>13 Mb</td>
<td>34 Mb</td>
<td>68 Mb</td>
<td>78 Mb</td>
<td>132.0 Mb</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>180</td>
<td>740</td>
<td>1,920</td>
<td>3,600</td>
<td>5,520</td>
<td>2,880</td>
</tr>
<tr>
<td>DSP Performance (symmetric FIR)</td>
<td>140GMACs</td>
<td>930GMACs</td>
<td>2,845GMACs</td>
<td>5,335GMACs</td>
<td>8,180 GMACs</td>
<td>4,266 GMACs</td>
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<tr>
<td>Transceiver Count</td>
<td>8</td>
<td>15</td>
<td>32</td>
<td>96</td>
<td>64</td>
<td>120</td>
</tr>
<tr>
<td>Transceiver Speed</td>
<td>3.2 Gb/s</td>
<td>6.6 Gb/s</td>
<td>12.5 Gb/s</td>
<td>28.05 Gb/s</td>
<td>16.3 Gb/s</td>
<td>32.75 Gb/s</td>
</tr>
<tr>
<td>Total Transceiver Bandwidth (full duplex)</td>
<td>50 Gb/s</td>
<td>211 Gb/s</td>
<td>600 Gb/s</td>
<td>2,784 Gb/s</td>
<td>2,085 Gb/s</td>
<td>5,885 Gb/s</td>
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<tr>
<td>Memory Interface (DDR3)</td>
<td>800</td>
<td>1,066</td>
<td>1,866</td>
<td>1,866</td>
<td>2,400</td>
<td>2,400</td>
</tr>
<tr>
<td>PCI Express® Interface</td>
<td>x1 Gen1</td>
<td>x4 Gen2</td>
<td>x8 Gen2</td>
<td>x8 Gen3</td>
<td>x8 Gen3</td>
<td>x8 Gen3</td>
</tr>
<tr>
<td>Analog Mixed Signal (AMS)XADC</td>
<td>-</td>
<td>XADC</td>
<td>XADC</td>
<td>XADC</td>
<td>System Monitor</td>
<td>System Monitor</td>
</tr>
<tr>
<td>Configuration AES</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>I/O Pins</td>
<td>576</td>
<td>500</td>
<td>1,200</td>
<td>3,632</td>
<td>832</td>
<td>1,456</td>
</tr>
<tr>
<td>I/O Voltage</td>
<td>1.2V – 3.3V</td>
<td>1.2V – 3.3V</td>
<td>1.2V – 3.3V</td>
<td>1.2V – 3.3V</td>
<td>1.0 – 3.3V</td>
<td>1.0 – 3.3V</td>
</tr>
</tbody>
</table>

**Digike.com (1/14/15):**

- Spartan-3A XC3S50A: $6.44
- Spartan-6 XC6SLX4: $11.48
- Artix-7 XC7A100T: $125.58; XC7A200T: $186.25
- Kintex-7 XC7K70T: $133.90; XC7K480T: $2,908.75
- Virtex7 XC7V2000T-G2FLG1925E: $39,452.40